GE
Intelligent Platforms

Hardware Reference

V7875*

Single Slot VME Single Board Computer

THE V7875 IS DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTION OF HAZARDOUS SUBSTANCE (ROHS) DIRECTIVE (2002/95/EC) CURRENT REVISION.

Publication No: 500-9300007875-000 Rev. D

imagination at work

Document History

Hardware Reference Manual Document Number: 500-9300007875-000 Rev. D

March 31, 2010

Waste Electrical and Electronic Equipment (WEEE) Returns

GE is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

GE will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

Table of Contents

List of Figures 5
List of Tables 6
Overview 8
1 • Installation and Setup 19
1.1 Unpacking Procedures. 19
1.2 Handling Precautions. 19
1.3 Mechanical Layout. 20
1.4 Hardware Setup. 22
1.4.1 Clear CMOS/Password and BIOS Boot Mode 27
1.5 Installation of V7875 into Chassis. 29
1.5.1 BIOS Setup 30
1.6 Installing or Removing a PMC Card. 30
1.7 Front Panel of V7875. 32
1.7.1 Connectors 32
1.7.2 PMC Filler Connectors 33
1.7.3 LEDs 33
1.8 BIOS Setup. 39
2 • Standard Features 40
2.1 V7875 Architecture. 40
2.1.1 Intel Core 2 Duo Processor, T9400 SV BGA CPU 40
2.1.2 GM45 GMCH 40
2.1.3 ICH9M I/O Controller hub 40
2.2 Physical Memory. 41
2.3 Memory Map. 42
2.4 I/O Port Map. 42
2.5 Interrupts. 44
2.5.1 System Interrupts 44
2.5.2 PCI Interrupts 47
2.5.3 PCI Device Interrupt Map 48
2.6 Integrated Peripherals. 50
2.7 Dual 10/100/1000 Ethernet via the Front Panel. 51
2.7.1 Boot ROM BIOS 51
2.7.2 Rear Optional VITA 41.3 Ethernet Controller 51
2.8 Video Graphics Adaptor. 52
2.8.1 VGA Interface 52
2.8.2 Digital Visual Interface (DVI-I) 53
2.9 Universal Serial Bus. 54
2.10 Notes Regarding PCIe x16 I/O. 54
3 • Embedded PC/RTOS Features 55
3.1 VME Bridge. 55
3.1.1 PCI-X To VME Bridge (Tsi148) Software Guidelines 56

3.2 Embedded Functions. 57
3.3 Timers. 58
3.3.1 General 58
3.3.2 Timer Enable Register 58
3.3.3 Timer Control Status Register (TCSR) 59
3.4 Timer 1 Value Register. 60
3.5 Timer 2 Value Register. 60
3.6 Timer 3 Value Register. 60
3.7 Timer 4 Value Register. 60
3.8 Timer 1 IRQ Clear (T1IC). 60
3.9 Timer 2 IRQ Clear (T2IC). 60
3.10 Timer 3 IRQ Clear (T3IC). 61
3.11 Timer 4 IRQ Clear (T4IC). 61
3.12 Watchdog Timer. 61
3.13 NVRAM. 61
3.14 CompactFlash Disk. 62
3.15 Remote Ethernet Booting. 62
3.15.1 Boot BIOS Features 62
Maintenance. 63
A • Appendix A: Connectors and Pinouts 64
A.1 VME P1/P2 Pinout 64
A.2 VME Connector Pinout (P1 and P2) 67
A.3 Optional Vita 41.3 Connector (P0) 68
A.4 Serial Connector RJ45 (J35) 69
A.5 USB Connectors and Pinout (J38 and J39) 69
A.6 DVI-I Connector and Pinout (J28) 70
A.7 Gigabit Ethernet Connector and Pinout (J32) 71
A.8 PMC Connector and Pinouts 72
A.8.1 PMC Connectors and Pinouts (J11) 72
A.8.2 PMC Connector and Pinouts (J12) 73
A.8.3 PMC Connector and Pinout (J13) 74
A.8.4 PMC Connector and Pinout (J14) 75
A.9 XMC Connector and Pinout (J15) 76
A.9.1 Board to Board Connector (P37) 76
B • Appendix B: AMI BIOS Setup Utility. 77
B.1 First Boot Menu 77
B.2 Main Menu 78
B.3 Advanced BIOS Setup Menu 79
B.4 PCI/PnP Setup Menu 80
B.5 Boot Setup Menu 81
B.6 Security Setup Menu 82
B.7 Chipset Setup Menu 83
B.8 Enabling and Disabling the Gigabit Ethernet boot-from-LAN BIOS 84
B.9 Exit Menu 85
C • Appendix C: Specifications and Physical Description 86

List of Figures

Figure 1 V7875 Board Block Diagram 13
Figure 1-1 V7875 Main Board 20
Figure 1-2 EXP237 Expansion Board 21
Figure 1-3 V7875 Connector Locations Top Assembly 23
Figure 1-4 V7875 Switch Locations Bottom Assembly 24
Figure 1-5 PMC Board Installation on V7875 31
Figure 1-6 0491 PMC Filler Module (Standard Features) Installation on V7875 31
Figure 1-7 0491 (Optional Features) Installation on V7875 32
Figure 1-8 Front Panel Layout/LED Status (Standard) 34
Figure 1-9 Front Panel Layout/LED Status (Optional) 35
Figure 1-10 Front Panel (Standard) from V7875 37
Figure 1-11 Front Panel (Optional) from V7875 38
Figure 2-1 Interrupt Logic 49
Figure A-1 V7875 Connector Location Top Assembly 65
Figure A-2 V7875 Switch Location Bottom Assembly 66
Figure A-3 VME Connectors 67
Figure A-4 Optional VITA 41.3 Connector 68
Figure A-5 Serial Connector (J35) 69
Figure A-6 USB Port 69
Figure A-7 DVI-I Connector and Pinout (J28) 70
Figure A-8 GbE Connector 71
Figure A-9 PMC Connector and Pinout (J11) 72
Figure A-10 Connector and Pinout (J12) 73
Figure A-11 Connector and Pinout (J13) 74
Figure A-12 Connector and Pinout (J14) 75

List of Tables

Table 1-1 V7875 Connectors, Headers and Switches. 25
Table 1-2 VMEbus System Controller Enable / Disable (S3) User Configurable 25
Table 1-3 VMEbus Mapping/SYSFAIL Generation - Switch (S6, S7) User Configurable 26
Table 1-4 VMEbus SYSRESET Enable\Disable Switch (S8) User Configurable 26
Table 1-5 G3 and G4 Ethernet Re-routing for VITA 41 boards (S10) 27
Table 1-6 JTAG PMC Bypassing and 82573 EEPROM Write Protection (S11) User Configurable 27
Table 1-7 Password Clear (S12)/BIOS Boot Mode Switch (S14) - Switch; User Configurable 27
Table 1-8 COM1 Configuration (RS232/RS422 Select) - Header (E14) User Configurable 28
Table 1-9 Battery Enable (S16) 28
Table 1-10 PN: 390-9300000026-000 Contents 33
Table 1-11 LED Indications 36
Table 2-1 V7875 Memory Map 42
Table 2-2 V7875 I/O Address Map 43
Table 2-3 V7875 Interrupt Line Assignment 44
Table 2-4 V7875 Interrupt Vector Table 45
Table 2-5 V7875 PCI Device Interrupt Mapping by the BIOS 48
Table 2-6 Partial List of Display Modes Supported for Analog 52
Table 2-7 Partial List of Display Modes Supported for Digital 53
Table 3-1 Embedded Functions Space Register. 57
Table 3-2 TCSR1 Bit Mapping 58
Table 3-3 Time Control Status Registers 59
Table 3-4 Timer Control Status Register Bit Map 59
Table 3-5 Timer x Clock Select 59
Table A-1 VME P1 and P2 Pinout 67
Table A-2 Optional Vita 1.3 Connector (P0) 68
Table A-3 Serial Connector Pinout (J35) 69
Table A-4 USB Connectors (J38/J39) 69
Table A-5 DVI-I Connector Pinout 70
Table A-6 Ethernet Connectors 10/100/1000 Mbit (J32) 71
Table A-7 PMC Connector Pinout (J11) 72
Table A-8 PMC Connector Pinout (J12) 73
Table A-9 PMC Connector and Pinout (J13) 74
Table A-10 PMC Connector and Pinout (J14) 75
Table A-11 XMC Connector and Pinout (J15) 76
Table B-1 AMI BIOS First Boot Menu. 77
Table B-2 AMI BIOS Main Menu 78
Table B-3 AMI BIOS Advanced Menu 79
Table B-4 AMI BIOS PCI/PnP Menu 80
Table B-5 AMI BIOS Boot Menu 81
Table B-6 AMI BIOS Security Menu 82

Table B-7 AMI BIOS Chipset Menu 83
Table B-8 AMI BIOS Exit Menu 85
Table C-1 V7875 General Specifications 86

Overview

Introduction

GE's V7875* is a VMEbus single board computer (SBC) in a single-slot, convection cooled, 6U VME form factor. The V7875 utilizes the advanced technology of Intel® Core™ 2 Duo Processor (T9400), Intel GM45 Express chipset, and ICH9M I/O controller hub. The GM45 Express chipset runs on a 1066 MHz front side bus with the Core 2 Duo processor. V7875 is compliant with VITA 1.5, VITA 39 (PCI-X on PMC), VITA 42.3 (PCIe on XMC) and VITA 41.3 (optional).

The V7875 provides further customer defined I/O capabilities with its design to support connection to a new high speed mezzanine product, the EXP237* XMC/PMC Expansion Board and the ACC-0603RC* Rear Transition Module (RTM). The EXP237 XMC/PMC expansion board provides three additional PCI-X XMC/PMC expansion sites to utilize.

A unique feature of the V7875 is the 0491* PMC Filler Module that fits in the onboard PMC/XMC site. The module fills the PMC bezel area when a PMC is not used and provides access to additional onboard I/O. The module adds connectivity on the front panel for two Gigabit Ethernet ports (only when VITA 41 is not used), and optionally, one eSATA port and one USB 2.0 port.

Desktop Features

- Up to 4 GByte DDR3 (1066 MHz) memory accomplished via a combination of memory down and SODIMM
- DVI-I port (front I/O) supporting digital and analog video output
- Dual Gigabit Ethernet (GbE) (front I/O)
- One RS232/422, RJ11, serial port (front I/O)
- A second serial support; Transmit/Receive support only (rear I/O)
- Four USB 2.0 ports (front I/O)
- Four USB 2.0 support (rear I/O)
- Supports two SATA connections (rear I/O)
- Real-Time clock/calendar
- Front panel reset switch
- 0491 PMC Filler Module with
  - Dual GbE RJ45
  - 2.0 port mini USB (optional)
  - One eSATA port (optional)

The Intel GM45 Express chipset allows the V7875 the capability of executing many of today's desktop operating systems such as Microsoft® Windows® XP, Windows Vista®, Linux® 2.6.x, and real-time operating systems like VxWorks® 6.x. The standard desktop features of the V7875 are described in **Chapter 2: Standard Features** of this manual.

- Intel Remote Boot Agent for all Ethernet ports
- Up to 8 GByte of bootable CompactFlash (optional)
- PMC site supporting XMC (VITA 42.3) and PCI-X (VITA 39) support
- PCIe board to board connector (x16) for expansion
- VME-2eSST VME protocol allows data transfers up to 320 MByte/s (VITA 1.5 VME)
- VME connectors are VITA 1.7 compliant
- 128 KByte NVRAM
- Software-selectable Watchdog Timer with reset
- Rear I/O support for PMC site, 46-pin P2 user I/O per VITA 35

The embedded features of the V7875 are described in **Chapter 3: Embedded PC/ RTOS Features**.

Designed for benign military/aerospace applications, the V7875 is suitable for use in a variety of commercial uses, such as: telecommunications, simulation, instrumentation, industrial control, process control and monitoring, factory automation, automated test systems, data acquisition systems and anywhere that the highest performance processing power for VME in a single or dual slot is desired.

Intel GM45 Express Chipset

The V7875 incorporates the latest Intel chipset technology, the GM45 Express chipset, consisting of the Intel GM45 Graphics memory Controller Hub (GMCH) and the Intel I/O Controller Hub (ICH) 9M. The ICH9 delivers optimal performance through high-bandwidth interfaces that include PCI Express, SerialATA and USB 2.0. The Intel GM45 Express chipset is designed for and validated with the Intel Core 2 Duo processor based on 45 nm technology that maximizes comprehensive validation and rapid deployment.

Key features:

- Optimized for the 45 nm T9400 processor at 2.53 GHz
- 1066 MHz Front Side Bus (FSB) delivering a high bandwidth connection between processor and chipset
- Support for video output options includes SVGA (up to 1600 x 1200) and DVI (up to 1024 x 768)
- Dual channel memory controller supports non-ECC 1066 MHz DDR3 SDRAM
- High-speed DMI architecture interface for communication between the memory controller (MCH) and ICH9M (I/O controller)

Software Support

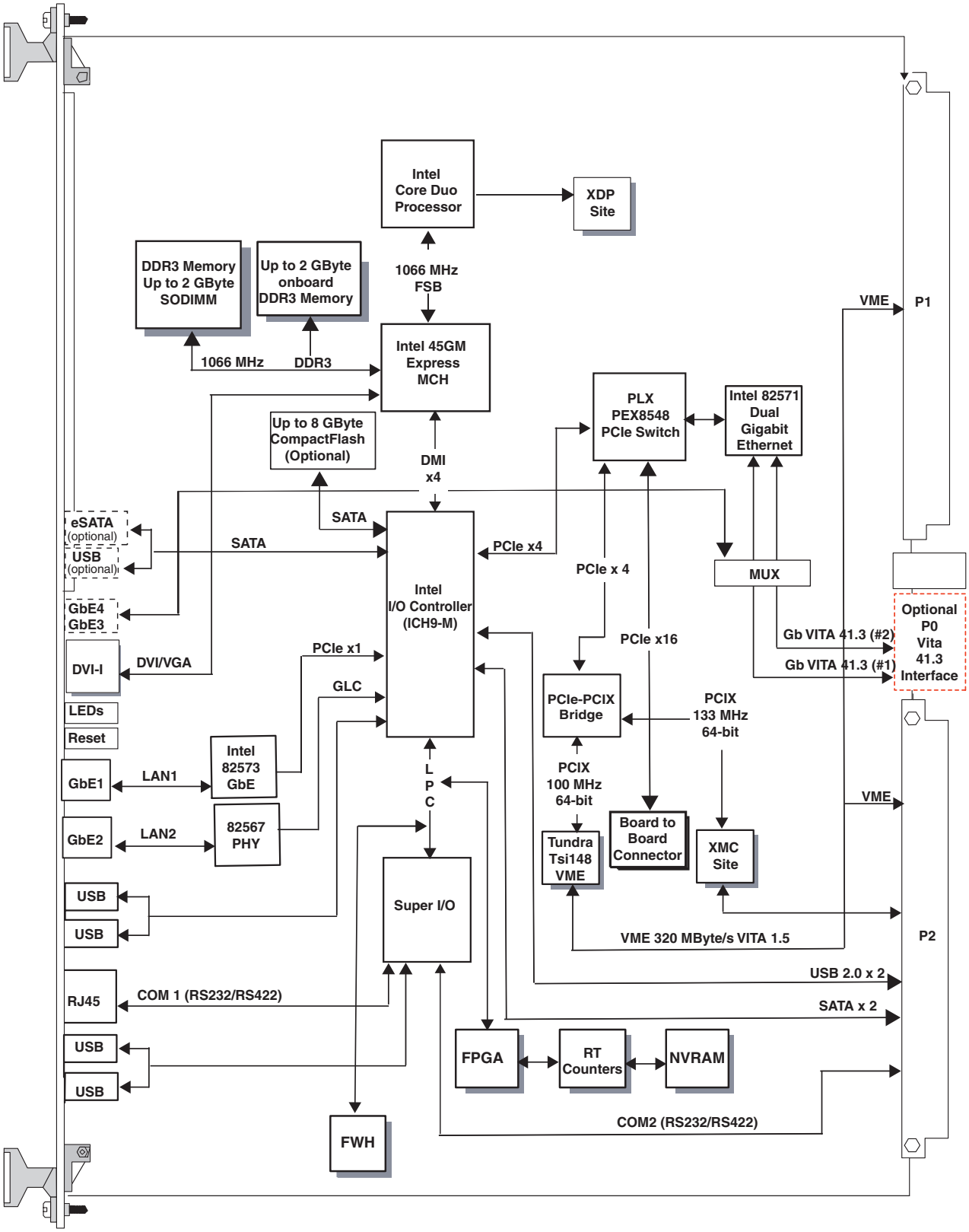
The V7875 has Tier 1 software support that includes Windows XP (32, 64, Embedded), Windows Vista (32, 64) and Linux (32, 64). All OS support includes dual core/SMP support to take advantage of the two cores in this design.

Other Software Functionality

Application Programming Interfaces (APIs) are provided to allow use of the real-time suite for all the OS.

V7875 Board Block Diagram

Figure 1 V7875 Board Block Diagram



References

Intel Penryn Processor for Montevina Platform: Electrical, Mechanical and Thermal Specification, Revision 0.7
March 2007

Montevina Platform Design Guide for Intel® Core™ 2 Duo Mobile Processor Built on 45-nm Process Technology, Mobile Intel® 45 Express Chipset and 82801IBM I/O Controller Hub (ICH9M) Revision 2
March 2008

Intel I/O Controller Hub 9 (ICH9) Family External Design Specification, Revision 2.0
June 2007

ACC-0603RC Product Specification
Doc. No. 800-9300800603-000
GE Intelligent Platforms
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616
www.ge-ip.com

ACC-0603RC VME Rear Transition Module Installation Guide
Doc. No. 522-9300800603-000
GE Intelligent Platforms
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616
www.ge-ip.com

Intel 82571EB/82572EI Gigabit Ethernet Controller Product Datasheet
December 2006, Revision 2.0

PCI Local Bus Specification, Rev. 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

CMC Specification, P1386/Draft 2.4a from:
IEEE Standards Department
Copyrights and Permissions
445 Hoes Lanes, P.O. Box 1331
Piscataway, NJ 08855-1331, USA

PMC Specification, P1386.1/Draft 2.4 from:
IEEE Standards Department
Copyrights and Permissions
445 Hoes Lanes, P.O. Box 1331
Piscataway, NJ 08855-1331, USA

For a detailed description and specification of the VME, please refer to:
VMEbus Specification Rev. C. and the VMEbus Handbook

VME International Trade Assoc. (VITA)
7825 East Gelding Dr.
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
(602) 951-0720 (FAX)

ANSI/VITA 1.0 - 1994 (R2002)
VME64 Standard

ANSI/VITA 1.1 - 1997
VME64 Extensions

ANSI/VITA 1.5 - 2003
VME 2eSST

ANSI VITA 1.7- 2003
Increased Current DIN Connector

ANSI/VITA 35-2000
PMC-P4 Pin Out Mapping to VME-PO and VME 64x-P2

ANSI/VITA 39-2003
PCI-X for PMC and Processor PMC

ANSI/VITA 41.3
VXS 1000Mb/s Baseband IEEE 802.3 Protocol Layer Standard

ANSI-VITA 42.3-2006
XMC PCI Express Protocol Layer Standard

PLX Technology PCI Express Switch (PEX8648) Data Boot
V0.95 April, 2008
www.plxtech.com

Tsi148 PCI/X-to-VME Bus Bridge User Manual
Doc. No. 80A3020-MA001-08
Tsi148 PCI/X-to-VME Bus Bridge Product Brief
Doc. No. 80A3020_FB001_06

Organization

This manual is composed of the following chapters and appendices:

Overview provides a general description of the V7875, References, general Safety Summary and symbols.

Chapter 1 Handling and Installation describes unpacking, handling and installing the hardware, as well as describing external interfaces.

Chapter 2 Standard Features describes the product's standard features and functionality.

Chapter 3 Embedded PC/RTOS Features describes capabilities beyond typical desktop computer systems.

Maintenance provides GE contact information relative to the care and maintenance of the unit.

Appendix A: Connector and Pinouts illustrates and defines the connectors included in the unit's I/O ports.

Appendix B: AMI BIOS Setup Utility describes the setup options in the system BIOS.

Appendix C: Specifications lists the hardware specifications for the V7875.

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

GE assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this system.
Use extreme caution when handling, testing and adjusting.

Warnings, Cautions and Notes

WARNING

WARNING denotes a hazard. It calls attention to a procedure, practice, or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

CAUTION denotes a hazard. It calls attention to an operating procedure, practice, or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE

NOTE denotes important information. It calls attention to a procedure, practice, or condition which is essential to highlight.

TIP

Tip denotes a bit of expert information.

LINK

This is link text.

1 • Installation and Setup

This chapter describes the unpacking, handling, installation and front panel of the V7875.

1.1 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Customer Care.

1.2 Handling Precautions

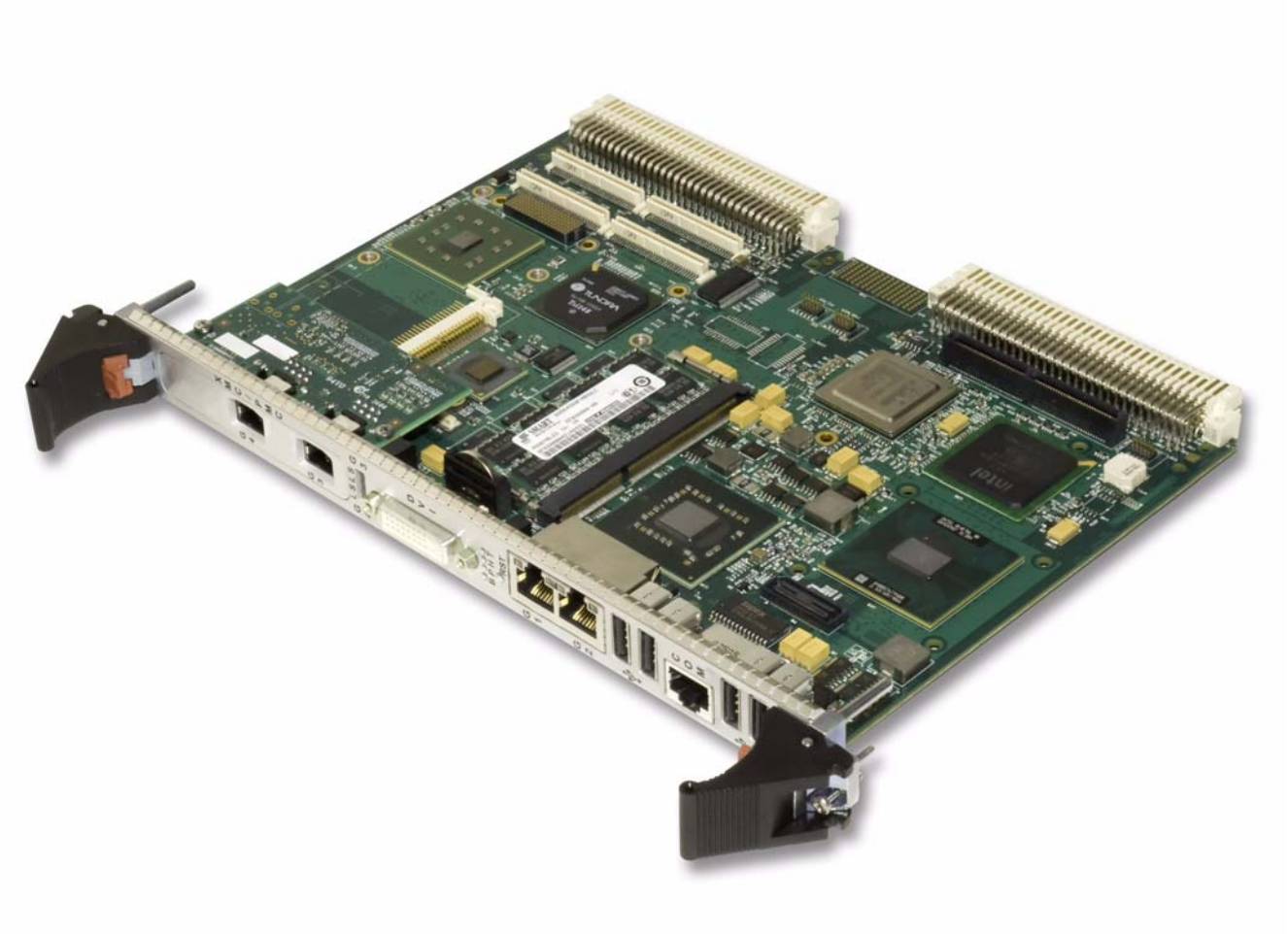
CAUTION

Some of the components assembled on GE products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

1.3 Mechanical Layout

The V7875 is constructed as a single 6U VME board with multiple optional modules or mezzanines. The main board is shown below:

Figure 1-1 V7875 Main Board



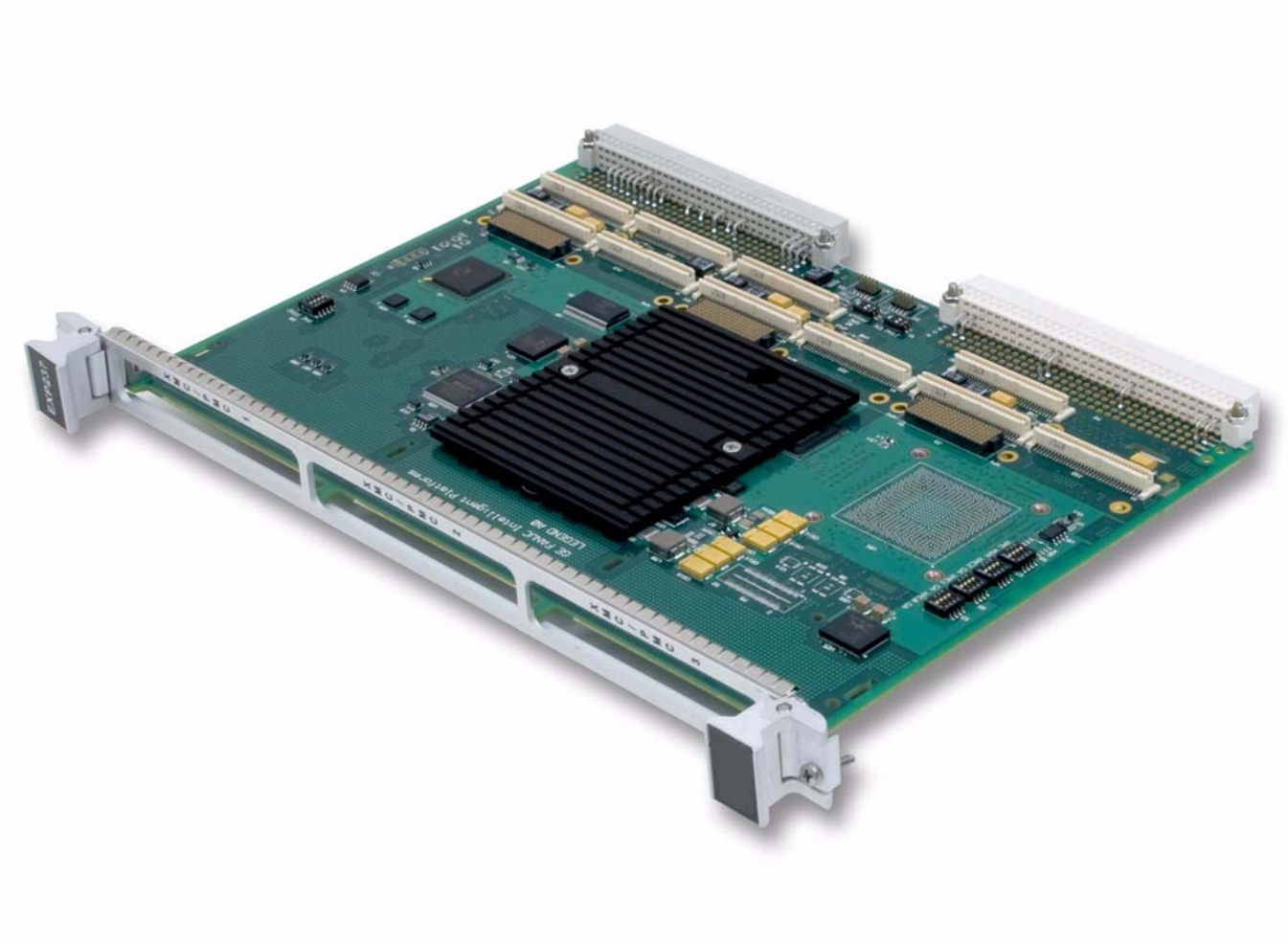
Modules are installed by the user and may be purchased separately from the product.

For installation instructions, see Section **1.5** ***Installation of V7875 into Chassis*** on page 29 and Section **1.6** ***Installing or Removing a PMC Card*** on page 30.

The V7875 is shipped with the 0491 PMC Filler Module for its single onboard XMC/PMC site. This module fills the PMC bezel area when a PMC is not used and provides access to additional onboard ethernet. The XMC/PMC filler is displayed in **Figure 1-6** page 31, **Figure 1-8** page 34, and **Figure 1-10** page 37.

For greater expansion capabilities, the V7875 offers a board-to-board connector supporting x16 lanes of PCIe. The expansion connector can support second-slot boards like the EXP237, which provides three XMC/PMC sites or two XMC/PMC sites with onboard high-performance video. The EXP237 is shown below:

Figure 1-2 EXP237 Expansion Board



1.4 Hardware Setup

The V7875 is factory populated with user-specified options as part of the V7875 ordering information. Contact Sales for ordering information at 1-800-322-3616. For option upgrades or for any type of repairs, contact customer care to receive a Return Material Authorization (RMA).

GE Customer Care is available at: (1-800-433-2682), 1-780-401-7700.

The V7875 is tested for system operation and shipped with factory-installed header jumpers and switches. The physical locations of the headers and connectors for the SBC with the PMC option are illustrated in **Figure 1-3 *V7875 Connector Locations Top Assembly*** on page 23. The definitions of the connectors, headers and switches are included in the Table Connectors, Headers and Switches in this Chapter.

All jumpers and switches marked *User Configured* in the following tables may be changed or modified by the user. All jumpers and switches marked *Factory Configured* should not be modified by the user.

Care must be taken when making jumper and switch modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit.

Modifying any jumper and switch not marked *User Configured* will void the Warranty and may damage the unit.

Figure 1-3 V7875 Connector Locations Top Assembly

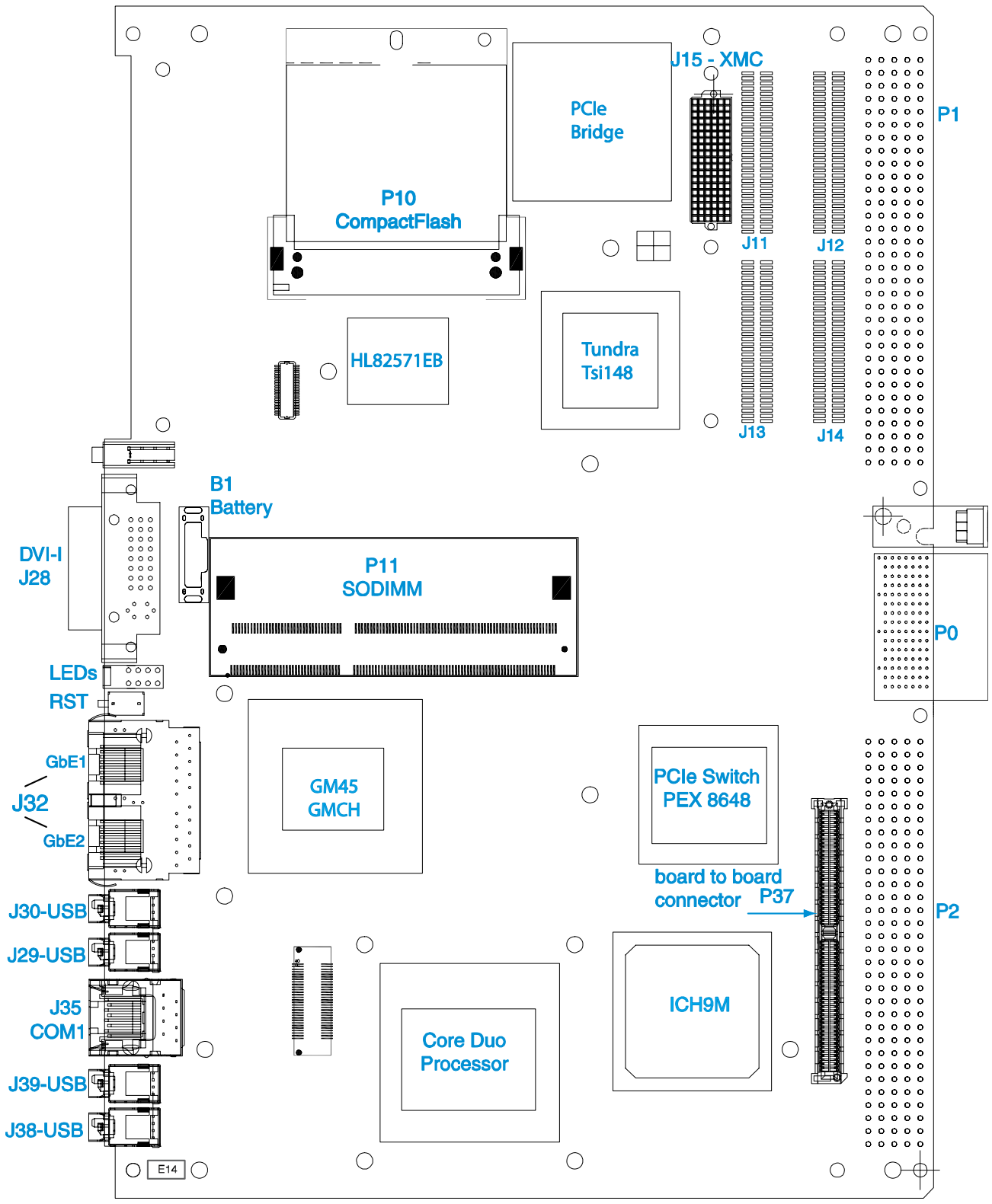


Figure 1-4 V7875 Switch Locations Bottom Assembly

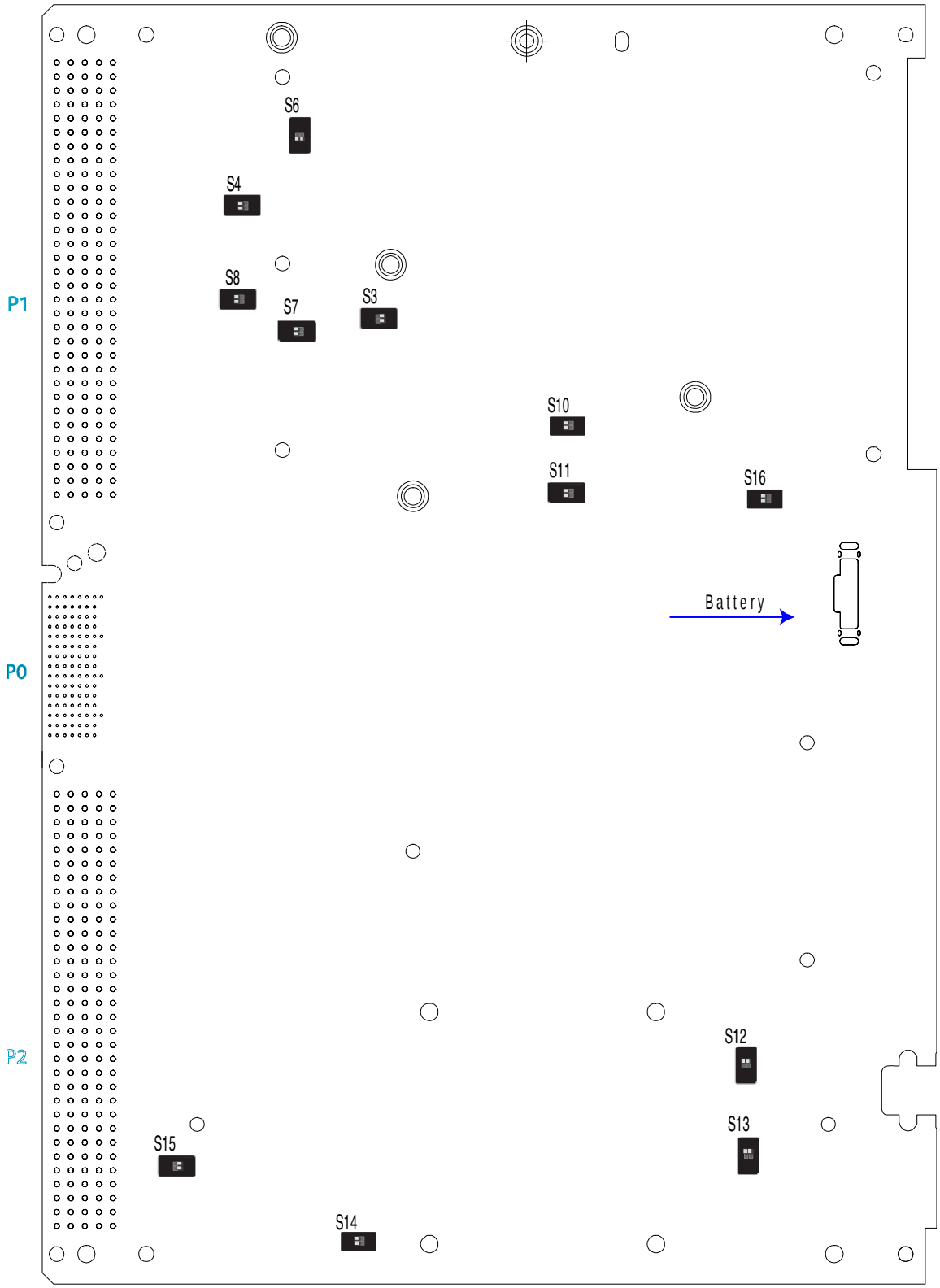


Table 1-1 V7875 Connectors, Headers and Switches

Connector	Function
P0, P38	VITA 41.3 Interface Connector (optional)
P1	VME Interface Connector
P2	USB 2.0, Serial ATA, COM2
P10	CompactFlash Socket
P11	SODIMM Socket
P37	Board to Board Connector for EXP237
J29, J30, J38 and J39	USB Ports
J32	Gigabit Ethernet Connectors (Dual RJ45)
J11, J12, J13 and J14	PMC Site Connectors
J15	XMC Site Connector
J35	Serial Port Connector (COM1)
J28	DVI-I
Header	**Function**
E14	COM1 Configuration
S15	COM1 Configuration
S13	COM1 (RS422 Termination)
Switches	**Function**
S3	VMEbus System Controller Enable and Disable
S6	VMEbus Mapping/Sysfail Generation
S7	VMEbus Mapping/Sysfail Generation
S8	VMEbus Sysreset Enable/Disable
S10	G3 and G4 Ethernet Re-routing for VITA 41 Boards
S11	JTAG PMC Bypassing and 82573 EEPROM Write Protection
S12	RTC Reset
S14	Boot Pause and SPI Write Protect
S16	Battery Enable

NOTE

The following tables display default settings in **bold**.

Table 1-2 VMEbus System Controller Enable / Disable (S3) User Configurable

Position	State
1-4 Off and 2-3 Off	**Auto Sense**
1-4 On and 2-3 Off	Syscon Enable
1-4 Off and 2-3 On	Syscon Disable
1-4 On and 2-3 On	Invalid

Table 1-3 VMEbus Mapping/SYSFAIL Generation - Switch (S6, S7) User Configurable

Select	Switch S6		Switch S7	
	1-4	2-3	1-4	2-3
CR/CSR disabled CRAT register, EN cleared by sysreset VCTRL register, SFAILAI cleared by sysreset GCTRL register, SFAILEN cleared by sysreset	**ON**	**X***	**ON**	**ON**
CR/CSR disabled CRAT.EN cleared by sysreset VCTRL.SFAILAI cleared by sysreset GCTRL register, SFAILEN set by sysreset	OFF	X	ON	ON
Auto Slot ID CRAT register, EN cleared by sysreset VCTRL register, SFAILAI set by sysreset GCTRL register, SFAILEN cleared by sysreset	ON	ON	OFF	ON
Illegal Configuration	OFF	X	OFF	ON
Auto Slot ID CRAT register, EN cleared by sysreset VCTRL register, SFAILAI set by sysreset, cleared 1ms after sysreset GCTRL register, SFAILEN cleared by sysreset	ON	OFF	OFF	ON
Geographical Addressing CRAT register, EN set by sysreset VCTRL register, SFAILAI cleared by sysreset GCTRL register, SFAILEN cleared by sysreset	ON	X	ON	OFF
Geographical Addressing CRAT register, EN set by sysreset VCTRL register, SFAILAI cleared by sysreset GCTRL register, SFAILEN set by sysreset	OFF	X	ON	OFF
Illegal Configuration	OFF	X	OFF	OFF
Default to Auto Slot ID CRAT register, EN cleared by sysreset VCTRL register, SFAILAI set by sysreset GCTRL register, SFAILEN cleared by sysreset	ON	ON	OFF	OFF
Default to Auto Slot ID CRAT register, EN cleared by sysreset VCTRL register, SFAILAI set by sysreset, cleared 1 ms after sysreset GCTRL register, SFAILEN cleared by sysreset	ON	OFF	OFF	OFF

* 'X' indicates a 'Don't Care' position. The switch can be in either position.

Table 1-4 VMEbus SYSRESET Enable\Disable Switch (S8) User Configurable

Position	State	Function
1-4	On	Enable VME SYSRESET Driver on VMEbus
2-3	On	Enable SYSRESET Receiver from VMEbus
1-4	**Off**	**Disable VME SYSRESET Driver on VMEbus**
2-3	**Off**	**Disable SYSRESET Receiver from VMEbus**

Table 1-5 G3 and G4 Ethernet Re-routing for VITA 41 boards (S10)

Position	State	Function
1-8	**On Factory Configured**	
2-7	**On Factory Configured**	
3-6	**Off Factory Configured**	
4-5	**On (User Configurable)**	G3 and G4 routed to P0*
4-5	Off (User Configurable)	G3 and G4 Routed to Front Panel*
4-5	**Off Factory Configured****	

*This setting only applies to VITA 41.3 Options to the board
**This setting applies to boards without the VITA 41.3 Options

Table 1-6 JTAG PMC Bypassing and 82573 EEPROM Write Protection (S11) User Configurable

Position	State	Function
1-4	**On**	**Write Protection to 82573 EEPROM Disabled**
1-4	Off	Write Protection to 82573 EEPROM Enabled
2-3	**On**	**Bypass PMC in JTAG Chain**
2-3	Off	Include PMC in JTAG Chain

1.4.1 Clear CMOS/Password and BIOS Boot Mode

NOTE

The BIOS has the capability of password protecting casual access to the unit's CMOS setup screens. The CMOS Clear switch allows the user to clear the password in the case of a forgotten password. This will also clear all CMOS settings and restore factory defaults.

Table 1-7 Password Clear (S12)/BIOS Boot Mode Switch (S14) - Switch; User Configurable

	Position	State	Function
Password Clear Switch S12	**2-3**	**Off**	**Normal**
	2-3	On	Clear CMOS/Password
	1-4	**Off Factory Configured**	
BIOS Boot Mode Switch S14	2-3	On	Boot with Post Errors
	2-3	**Off**	**Boot Halt on Post Errors**
	1-4	**Off Factory Configured**	

To clear the CMOS password:

1. Turn off power to the unit.
2. Move switch S12 position 1 to On.
3. Wait approximately 5 seconds.
4. Move switch S12 position 1 to Off.
5. Power up the unit.

When power is reapplied to the unit, the CMOS password will be cleared, and the CMOS will be set to its defaults.

Table 1-8 COM1 Configuration (RS232/RS422 Select) - Header (E14) User Configurable

Select	S15 State	E14 Position	S13 State
RS232	**1-4 ON and 2-3 ON**	**1-3, 4-6**	**1-4 and 2-3 both OFF**
RS422 w/Termination	1-4 and 2-3 both OFF	1-3, 2-4	1-4 and 2-3 both ON
RS422 w/o Termination	1-4 and 2-3 both OFF	1-3, 2-4	1-4 and 2-3 both OFF

Table 1-9 Battery Enable (S16)

Position	State
1-4 and 2-3	**On**

1.5 Installation of V7875 into Chassis

The V7875 conforms to the VME physical specification for a 6U board. The V7875 can be used as the system controller or as a peripheral board. It can be plugged directly into any standard chassis accepting either type of board.

CAUTION

Do not install or remove the board while power is applied.

The following steps describe the GE recommended method for installation and powerup of the V7875:

1. Make sure power to the equipment is off.
2. Connect a PMC or an XMC module to the V7875 (if it is to be used) prior to board installation. See **1.6 *Installing or Removing a PMC Card*** on page 30. Refer to the Product Manual for the XMC/PMC module for configuration and setup.

NOTE

Air flow as measured at the output side of the heatsink is to be greater than 450 LFM.

3. Choose chassis slot. The V7875 must be attached to a P1/P2 VME backplane. If the V7875 has the optional P0 connector, choose an appropriate VXS chassis. In many cases, a V7875 with a P0 connector installed will not plug into a standard VME backplane.
   a. If the V7875 is to be the VME system controller, choose the first VME slot.
   b. If a different board is the VME system controller, choose any slot ***except*** Slot One.

      The V7875 does not require jumpers for enabling/disabling the system controller function.

      See S3 switch settings to force system controller settings
4. Insert the V7875 into a VME chassis system controller or peripheral slot.
   a. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector.
   b. Use the ejector handles to firmly seat the board.
5. Access all needed peripherals from the front panel or the rear I/O. Each connector is clearly labeled. Detailed pinouts are in ***Appendix A: Connectors and Pinouts***.
6. Connect a keyboard and mouse if the system has not been previously configured.
7. Refer to Section **3.14 *CompactFlash Disk,*** page 62 for setup details, if applicable. The V7875 features an optional CompactFlash Disk resident on the board.
8. If an external drive module is installed, the BIOS Boot Setup Menu or F11 first boot key may be used to select booting from the drive. Refer to Appendix B Section **B.5 *Boot Setup Menu*** on page 81 and Section **B.1 *First Boot Menu*** on page 77.
9. Install the operating system according to the manufacturer's instructions, if a drive module is present.

1.5.1 BIOS Setup

The V7875 has an onboard BIOS Setup program that controls many configuration options. These options are saved in a special non-volatile, battery-backed memory chip and are collectively referred to as the board's "CMOS Configuration." The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied. The CMOS clear switch, S12 , clears BIOS settings to factory defaults.

Details of the V7875 BIOS setup program are included in ***Appendix B: AMI BIOS Setup Utility***.

1.6 Installing or Removing a PMC Card

The V7875 incorporates PMC expansion sites that support the PCI-X bus. The PMC site is on a private PCI-X bus segment allowing for maximum data transfer rates of 1064 MByte/s between the processors and the PMC device. The PMC sites are capable of up to 133 MHz operation and support 3.3 V (not 5 V) signaling (or VIO). They are compatible with the earlier PCI interface versions (33/66 MHz, 32/64-bit).

NOTE

For best performance, PMC card drivers should use DMA.

NOTE

The V7875 does not support 5 V signaling (or VIO) only PMC cards, and has the PMC keying pin installed accordingly. Removal of the PMC keying pin could result in damage to the board.

The V7875 is shipped with the 0491 PMC Filler Module as shown in **Figure 1-6** page 31.

The following procedure is applicable for both removal and installation of PMC modules and fully populated PMC cards. See **Figure 1-5, *PMC Board Installation on V7875,*** on page 31 and **Figure 1-6 *0491 PMC Filler Module (Standard Features) Installation on V7875*** on page 31.

1. Remove the mezzanine screws.
2. Separate the mezzanine connector while lifting and rotating the mezzanine board. Pull away from the front panel.
3. Remove the PMC modules by removing two mounting screws per module. This step will be necessary when initially installing a PMC card into a V7875.

Follow the reverse sequence to install a PMC card or a PMC module.

Figure 1-5 PMC Board Installation on V7875

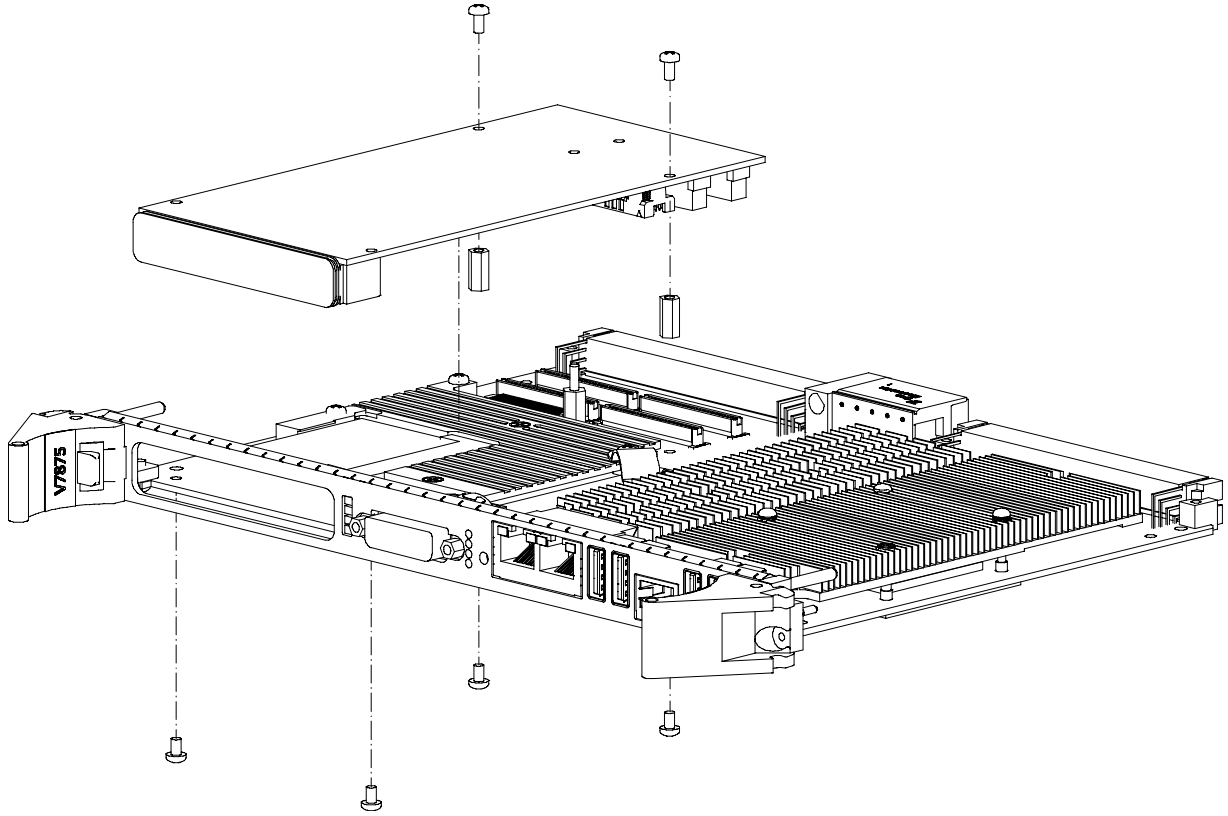


Figure 1-6 0491 PMC Filler Module (Standard Features) Installation on V7875

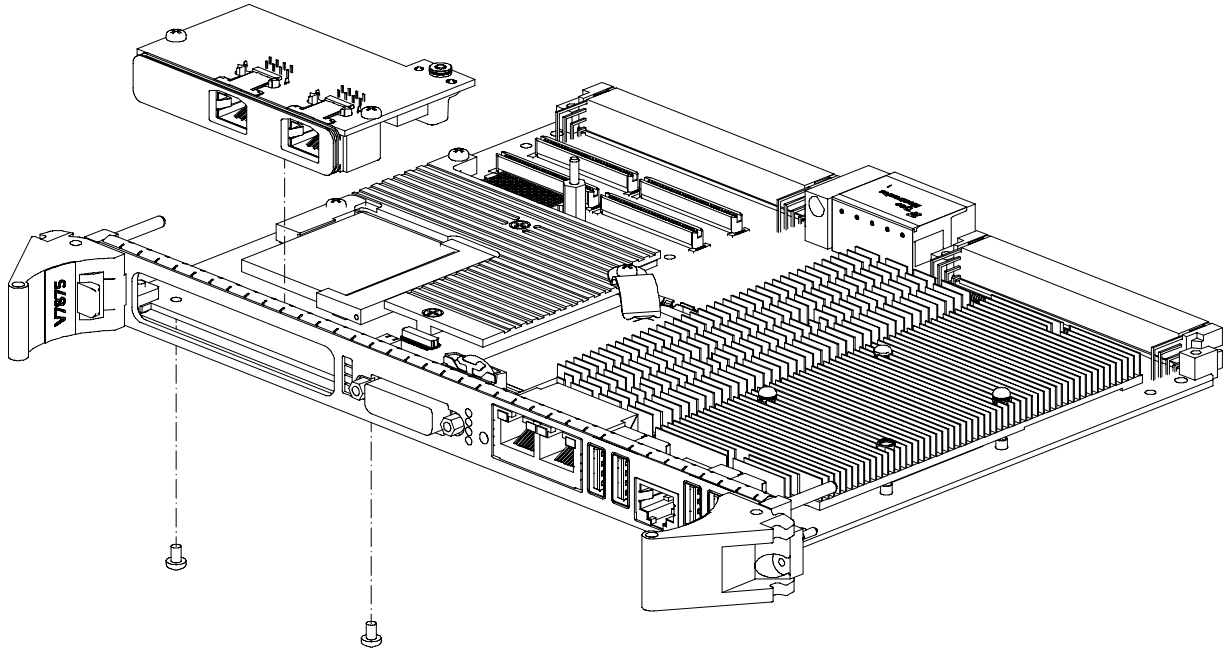
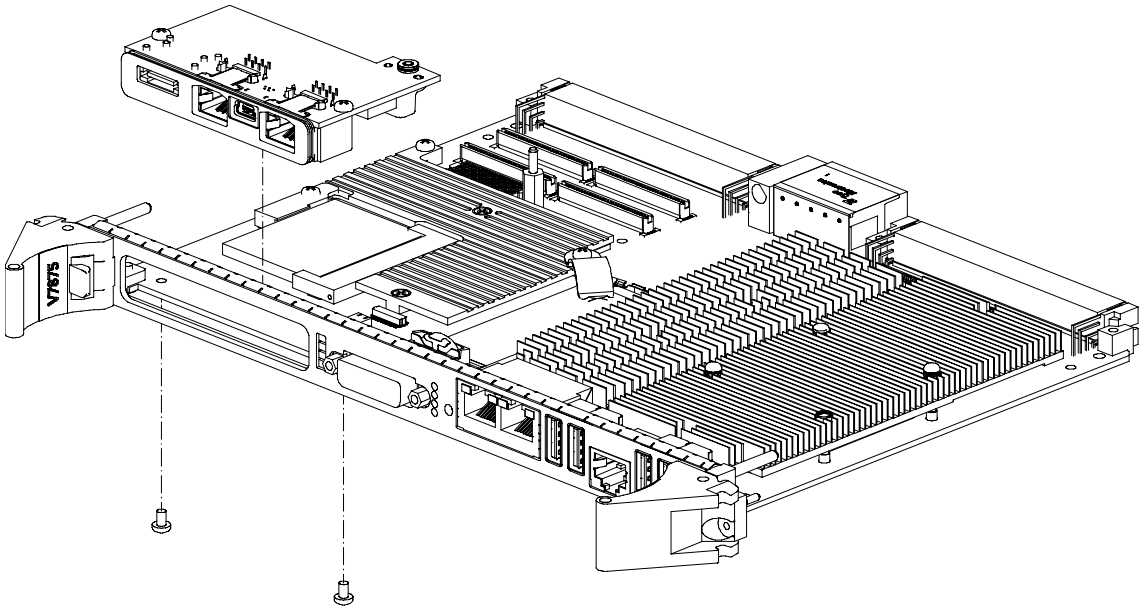


Figure 1-7 0491 (Optional Features) Installation on V7875



1.7 Front Panel of V7875

1.7.1 Connectors

The V7875 provides front-panel access to the XMC/PMC expansion site, the DVI-I connector, two GbE connectors, the manual reset switch, COM1 port, four USB ports and the status LEDs. A drawing of the V7875 front panel is shown in **Figure 1-8 *Front Panel Layout/LED Status (Standard)*** on page 34.

The front panel connectors and indicators are labeled as follows:

- DVI DVI-I connector
- BPHT Status LEDs
- RST Manual reset switch
- G1 GbE Connector, Front
- G2 GbE Connector, Front
- COM COM port
- USB USB connectors*

NOTE

*The use of USB to PS2 adapters is not supported.

The V7875 provides rear I/O support for VME with 2eSST 320MB/s, Optional VXS support (VITA 41.3), two USB 2.0 ports, COM2 (RS232/RS422), and two SATA drives. These signals are accessed by the use of a rear transition module (RTM) such as the the ACC-0603RC, which terminates the signals into industry standard connectors. The front panel connectors, including connector pinouts and orientation for the V7875, are defined in ***Appendix A: Connectors and Pinouts***.

NOTE

RTMs may not support all available V7875 rear I/O mentioned above. RTM connections are defined in the appropriate RTM Installation Guide.

1.7.2 PMC Filler Connectors

The 0491 PMC Filler Module provides additional front-panel connectors:

- G3, G4 GbE Connectors
- miniUSB (optional)
- eSATA (optional)

The optional 0491 PMC Filler Module's USB port is a mini-USB type. Customers may order a cable adapter kit (PN: 390-9300000026-000) which contains the following adapters to connect to the miniUSB or eSATA connectors if this option is chosen:

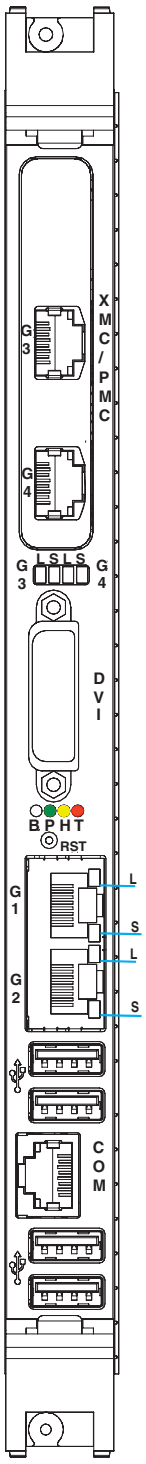
Table 1-10 PN: 390-9300000026-000 Contents

QTY	Description
1	Adapter: mini-USB to Female USB type A
1	Cable: eSATA to SATA, 1.8-2m length

1.7.3 LEDs

See **Figure 1-8** ***Front Panel Layout/LED Status (Standard)*** on page 34 to view the definitions of the various LEDs on the front panel.

Figure 1-8 Front Panel Layout/LED Status (Standard)



XMC/PMC Site

When the PMC is not used, the 0491 PMC Filler Module provides access to onboard I/O. The Standard Front Panel of the PMC Module is displayed with G3 and G4 GbE Connectors.

Rear GbE Ethernet LEDs (G4 and G3)

Ethernet Activity: **L** - Blinks green when the Ethernet is linked and active. It remains steady if the Ethernet is linked, with no activity.

Ethernet Speed: **S** - Indicates at which speed the Ethernet is running:

10Base-T: LED is off
100Base-TX: Yellow LED
1000Base-T: Green LED

Status LEDs (BPHT)

LED **B** *Boot Done* - Indicates BIOS powerup self test (POST) is in progress, LED is lit (Red LED). Once POST completes, LED turns off. Once booting completes, "VMESYSFAIL" causes the LED to turn on.

LED **P** *Power Good* - Indicates when all onboard power is within tolerance (Green LED).

LED **H** *Drive Activity* - Indicates hard drive activity on either one of the SATA or CompactFlash drives (Yellow LED).

LED **T** *Thermal Alerts* - Indicates when the temperature of the CPU exceeds the operating temperature (Red LED).

RST *Reset* - Allows the system to be reset from the front panel.

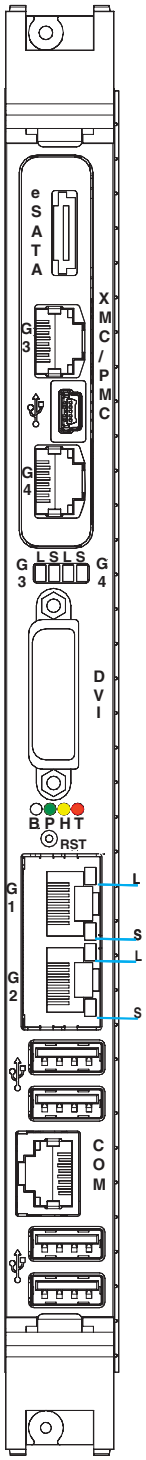
Front GbE Ethernet LEDs (G1 and G2)

Ethernet Activity: **L** - Blinks green when the Ethernet is linked and active. It remains steady if the Ethernet is linked, with no activity.

Ethernet Speed: **S** - Indicates at which speed the Ethernet is running:

10Base-T: LED is off
100Base-TX: Yellow LED
1000Base-T: Green LED

Figure 1-9 Front Panel Layout/LED Status (Optional)



XMC/PMC Site

When the PMC is not used, the 0491 PMC Filler Module provides access to onboard I/O. The Optional Front Panel of the PMC Module is displayed with G3 and G4 GbE and the optional eSATA port and miniUSB port.

GbE Ethernet LEDs (G4 and G3)

Ethernet Activity: **L** - Blinks green when the Ethernet is linked and active. It remains steady if the Ethernet is linked, with no activity.

Ethernet Speed: **S** - Indicates at which speed the Ethernet is running:

10Base-T: LED is off
100Base-TX: Yellow LED
1000Base-T: Green LED

Status LEDs (BPHT)

LED **B** *Boot Done* - Indicates BIOS powerup self test (POST) is in progress, LED is lit (Red LED). Once POST completes, LED turns off. Once booting completes, "VMESYSFAIL" causes the LED to turn on.

LED **P** *Power Good* - Indicates when all onboard power is within tolerance (Green LED).

LED **H** *Drive Activity* - Indicates hard drive activity on either one of the SATA or CompactFlash drives (Yellow LED).

LED **T** *Thermal Alerts* - Indicates when the temperature of the CPU exceeds the operating temperature (Red LED).

RST *Reset* - Allows the system to be reset from the front panel.

Front GbE Ethernet LEDs (G1 and G2)

Ethernet Activity: **L** - Blinks green when the Ethernet is linked and active. It remains steady if the Ethernet is linked, with no activity.

Ethernet Speed: **S** - Indicates at which speed the Ethernet is running:

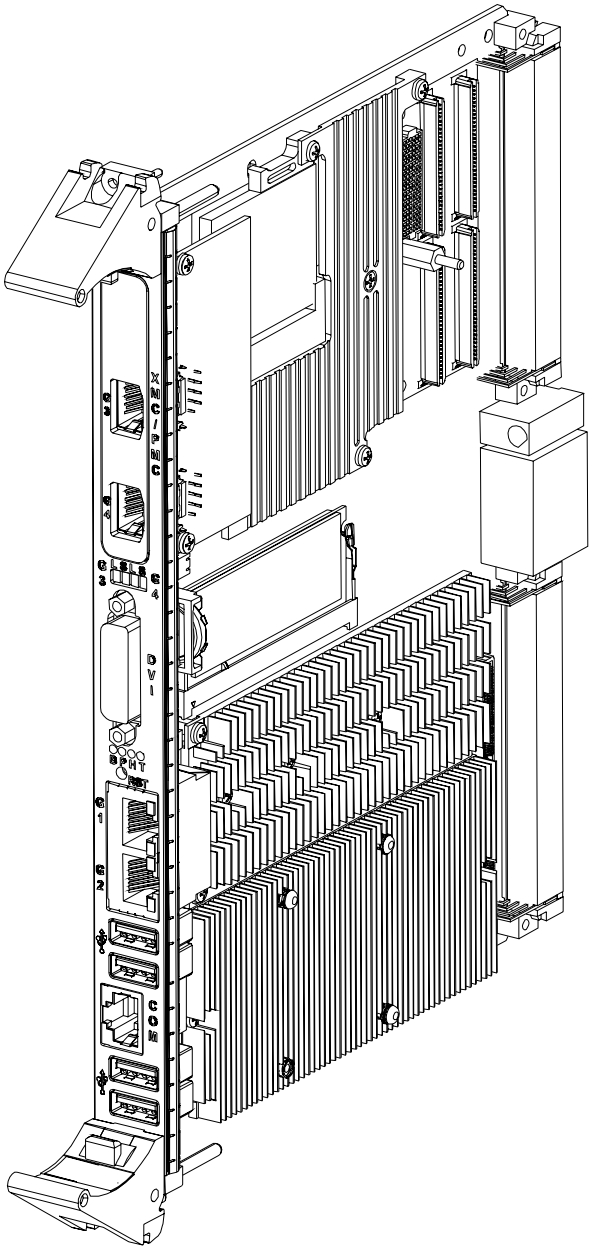
10Base-T: LED is off
100Base-TX: Yellow LED
1000Base-T: Green LED

The front panel LEDs are used to indicate various modes of operational status. A summary of these indications is in the following Table:

Table 1-11 LED Indications

State	Indication
VME SYSFAIL	Red "B" LED illuminates with each VME SYSFAIL 'seen' on the bus. The LED will remain on as long as the failure lasts.
Normal Operation	LED B = Off (out of Power On Self Test - POST) LED P = On (power is good) LED H = Off, or Flashing (hard drive activity) LED T = Off (temperature of CPU is within operating limits)

Figure 1-10 Front Panel (Standard) from V7875



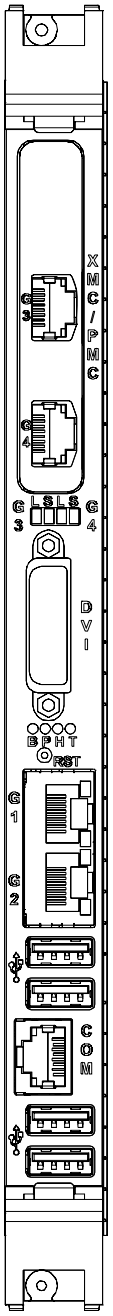
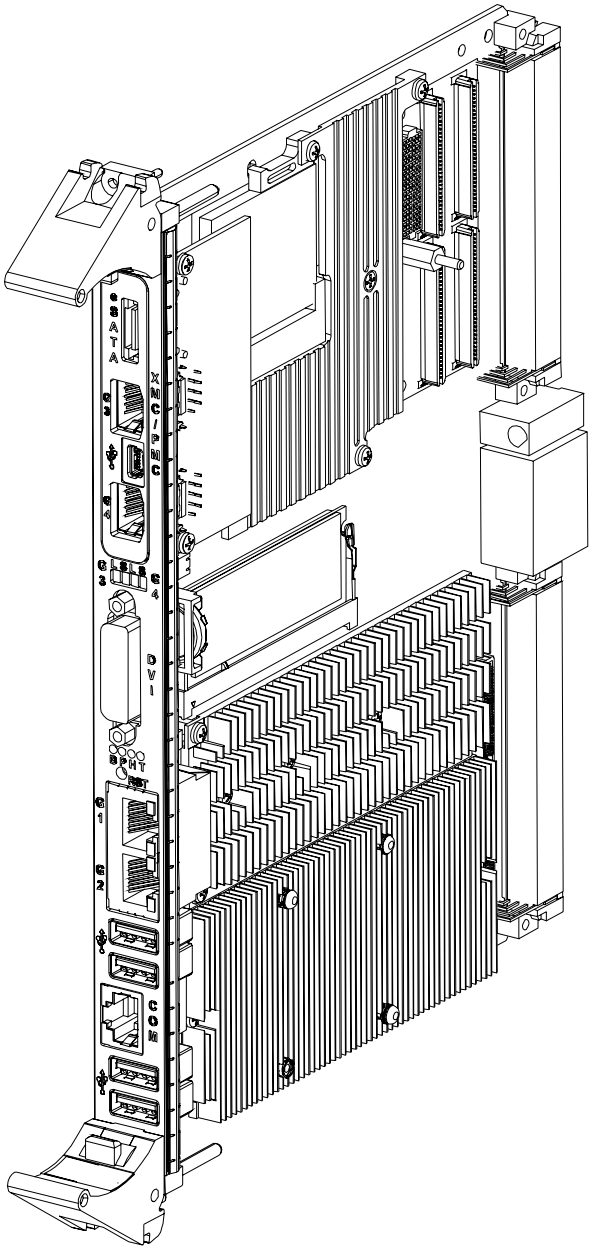
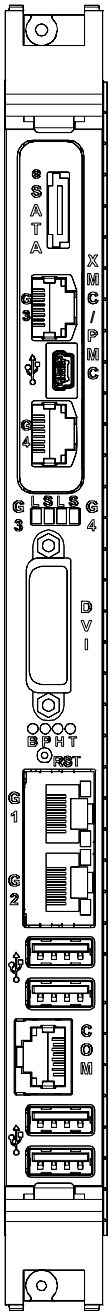


Figure 1-11 Front Panel (Optional) from V7875





1.8 BIOS Setup

The V7875 has an onboard BIOS Setup program (AMI BIOS) that controls many configuration options. These options are saved in non-volatile, battery-backed memory and are collectively referred to as the board's "CMOS Configuration." The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied. The CMOS clear switch, S12 , clears BIOS settings to factory defaults.

See ***Appendix B: AMI BIOS Setup Utility*** for setup details.

2 • Standard Features

The V7875 is a single board computer loaded with the Intel Core 2 Duo processor and compatible with modern industry standard desktop systems. The V7875, therefore, retains industry standard memory and I/O maps along with a standard interrupt architecture. The integrated peripherals described in this section (such as serial ports, USB ports, CompactFlash, video controller and Ethernet controller) are all memory mapped the same as similarly equipped desktop systems, ensuring compatibility with modern operating systems.

The following sections describe the standard features of the V7875.

2.1 V7875 Architecture

The V7875 is comprised of the Intel Core 2 Duo Processor, GM45 Express chipset and ICH9M I/O controller hub.

2.1.1 Intel Core 2 Duo Processor, T9400 SV BGA CPU

The V7875 incorporates the latest Intel Core 2 Duo Processor on 45 nanometer process technology. This processor is the next generation high-performance, low-power mobile processor based on the Intel Core micro architecture and has the following new features:

- 1066 MHz Source-synchronous Front Side Bus (FSB)
- Intel Trusted Execution Technology
- SSE4.1 Instructions
- New Deep Power down technology (also called C6 state) low power state which further reduces power consumption when the processor is idle
- Enlarged 6 MByte L2 cache memory

2.1.2 GM45 GMCH

The GM45 Express chipset Graphics Memory Controller Hub (GMCH) is equipped with the following new features:

- Gen 5.0 integrated Graphics Engine
- Support for DDR3 at 1066 MHz
- High bandwidth (x16) PCIe expansion bus

2.1.3 ICH9M I/O Controller hub

The ICH9M I/O controller hub (ICH9M) has the following enhancements:

- Eleven USB ports (nine available)
- Four SATA ports (three available; one used for the CompactFlash)
- CPU Deep Power Down Technology (also called C6) state support

2.2 Physical Memory

The V7875 provides DDR3 (1066) Synchronous DRAM (SDRAM) as onboard system memory. Memory can be accessed as bytes, words or longwords.

The V7875 has a maximum memory configuration of 4 GByte of DDR3 SDRAM memory.

This configuration calls for a 2 GByte SODIMM (one 200-pin SODIMM DDR3 module) and 2 GByte of onboard memory. The SDRAM is dual-ported to the VME through the PCI-to-VME bridge and is addressable by the local processor, as well as the VME slave interface by another VME master.

CAUTION

Caution must be used when sharing memory between the local processor and the VME to prevent a VME deadlock and to prevent a VME master from overwriting the local processor's operating system.

The V7875 includes 128 KByte of non-volatile SRAM which can be accessed by the CPU at any time, and is used to store system data that must not be lost during power-off conditions.

2.3 Memory Map

Memory Map - Tsi148 Based PCI-to-VME Bridge

The memory map for the V7875 is shown in Table 2-1. All systems share this same memory map.

Table 2-1 V7875 Memory Map

Mode	Memory Address Range	Size	Description
Protected Mode	$FFFF 0000 - $FFFF FFFF	64 KByte	ROM BIOS Image
	TOLM*** - $FFFF FFFF	X.X GByte	Unused*
	$0010 0000 - TOLM	X.X GByte	Reserved for **
			Onboard Extended Memory (not filled on all systems)
Real Mode	$E0000 - $FFFFF	128 KByte	
	$C0000 - $DFFFF	128 KByte	
	$A0000 - $BFFFF	128 KByte	
	$00000 - $9FFFF	640 KByte	

* BIOS will map PCI devices, PCI-based NVRAM, in this area.

** This space can be allocated as shared memory (for example, between the BGA CPU and VME Master). Note that if a PMC board is loaded, the expansion BIOS may be placed in this area.
***TOLM - Top of Lower Memory

2.4 I/O Port Map

Like a desktop system, the V7875 includes special input/output instructions that access I/O peripherals residing in I/O addressing space (separate and distinct from memory addressing space). Locations in I/O address space are referred to as ports. When the CPU decodes and executes an I/O instruction, it produces a 16-bit I/O address on lines A00 to A15 and identifies the I/O cycle with the M/I/O control line. Thus, the CPU includes an independent 64 KByte I/O address space, which is accessible as bytes, words or longwords.

Standard hardware circuitry reserves only 1,024 byte of I/O addressing space from I/O $000 to $3FF for peripherals. All standard PC I/O peripherals, such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly; adjusting these I/O ports directly is not normally necessary.

The assigned and user-available I/O addresses are summarized in the I/O Address Map Table below:

Table 2-2 V7875 I/O Address Map

I/O Address Range	Size In Bytes	HW Device	PC/AT Function
$000 - $00F	16		DMA Controller 1
$010 - $01F	16		Reserved
$020 - $021	2		Master Interrupt Controller
$022 - $03F	30		Reserved
$040 - $043	4		Programmable Timer
$044 - $05F	30		Reserved
$060 - $064	5		Keyboard, Speaker, System Configuration
$065 - $06F	11		Reserved
$070 - $071	2		Real-Time Clock
$072 - $07F	14		Reserved
$080 - $08F	16		DMA Page Registers
$090 - $091	2		Reserved
$092	1		Alt. Gate A20/Fast Reset Register
$093 - $09F	11		Reserved
$0A0 - $0A1	2		Slave Interrupt Controller
$0A2 - $0BF	30		Reserved
$0C0 - $0DF	32		DMA Controller 2
$0E0 - $16F	142		Reserved
$170 - $177	8	ICH9-M	Secondary Hard Disk Controller
$178 - $1EF	120		User I/O
$1F0 - $1F7	8	ICH9-M	Primary Hard Disk Controller
$1F8 - $277	128		User I/O
$278 - $27F	8	I/O Chip	Reserved
$280 - $2E7	104		Reserved
$2E8 - $2EE	7	UART*	COM4 Serial I/O*
$2EF - $2F7	9		User I/O
$2F8 - $2FE	7	Super-I/O Chip	COM2 Serial I/O (16550 Compatible)
$2FF - $36F	113		Reserved
$370 - $377	8	Super-I/O Chip*	Secondary Floppy Disk Controller*
$378 - $37F	8	Super-I/O Chip	Reserved
$380 - $3E7	108		Reserved
$3E8 - $3EE	7	UART*	COM3 Serial I/O*
$3F0 - $3F7	8	Super-I/O Chip*	Primary Floppy Disk Controller*
$3F8 - $3FE	7	Super-I/O Chip	COM1 Serial I/O (16550 Compatible)
$3FF - $4FF	256		Reserved
$500 - 5FF	256		Reserved
$600 - 61F	32	Embedded Timers and NVRAM	Embedded function
$620 - CFF	1760		Reserved

* While these I/O ports are reserved for the listed functions, they are not implemented on the V7875. They are listed here to make the user aware of the standard PC usage of these ports.

2.5 Interrupts

2.5.1 System Interrupts

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The sixteen maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 2-3, **V7875 Interrupt Line Assignment** along with their functions. Table 2-4, **V7875 Interrupt Vector Table** details the vectors in the interrupt vector table. The interrupt number in HEX and decimal are also defined for real and protected mode in Table 2-4.

The interrupt hardware implementation on the V7875 is standard for computers built around the PC architecture, which evolved from the IBM PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the PIC. The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This architecture is represented in **Figure 2-1** ***Interrupt Logic*** on page 49.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

Table 2-3 V7875 Interrupt Line Assignment

IRQ	AT Function	Comments
NMI	Parity Errors (Must be enabled in BIOS Setup)	Used by V7875 PCI bus Interface
0	System Timer	Set by BIOS Setup
1	Keyboard	Set by BIOS Setup
2	Duplexed to IRQ9	
3	COM2	
4	COM1	
5	Unused	
6	Floppy Controller	
7	Unused	
8	Real-Time Clock	
9	Old IRQ2	SVGA or Network I/O
10	Not Assigned	Determined by BIOS
11	Not Assigned	Determined by BIOS
12	Mouse	
13	Math Coprocessor	
14	AT Hard Drive	
15	CompactFlash	

Table 2-4 V7875 Interrupt Vector Table

Interrupt No				
HEX.	DEX	IRQ Line	Real Mode	Protected Mode
00	0		Divide Error	Same as Real Mode
01	1		Debug Single Step	Same as Real Mode
02	2	NMI	Memory Parity Error, VME Interrupts	Same as Real Mode (Must be enabled in BIOS Setup)
03	3		Debug Breakpoint	Same as Real Mode
04	4		ALU Overflow	Same as Real Mode
05	5		Print Screen	Array Bounds Check
06	6			Invalid OpCode
07	7			Device Not Available
08	8	IRQ0	Timer Tick	Double Exception Detected
09	9	IRQ1	Keyboard Input	Coprocessor Segment Overrun
0A	10	IRQ2	BIOS Reserved	Invalid Task State Segment
0B	11	IRQ3	COM2 Serial I/O	Segment Not Present
0C	12	IRQ4	COM1 Serial I/O	Stack Segment Overrun
0D	13	IRQ5	Unassigned	Unassigned
0E	14	IRQ6	Floppy Disk Controller	Page Fault
0F	15	IRQ7	Unassigned	Unassigned
10	16		BIOS Video I/O	Coprocessor Error
11	17		System Configuration Check	Same as Real Mode
12	18		Memory Size Check	Same as Real Mode
13	19		XT Floppy/Hard Drive	Same as Real Mode
14	20		BIOS Comm I/O	Same as Real Mode
15	21		BIOS Cassette Tape I/O	Same as Real Mode
16	22		BIOS Keyboard I/O	Same as Real Mode
17	23		BIOS Printer I/O	Same as Real Mode
18	24		ROM BASIC Entry Point	Same as Real Mode
19	25		Bootstrap Loader	Same as Real Mode
1A	26		Time of Day	Same as Real Mode
1B	27		Control/Break Handler	Same as Real Mode
1C	28		Timer Control	Same as Real Mode
1D	29		Video Parameter Table Pntr	Same as Real Mode
1E	30		Floppy Parm Table Pntr	Same as Real Mode
1F	31		Video Graphics Table Pntr	Same as Real Mode
20	32		DOS Terminate Program	Same as Real Mode
21	33		DOS Function Entry Point	Same as Real Mode
22	34		DOS Terminate Handler	Same as Real Mode
23	35		DOS Control/Break Handler	Same as Real Mode
24	36		DOS Critical Error Handler	Same as Real Mode
25	37		DOS Absolute Disk Read	Same as Real Mode
26	38		DOS Absolute Disk Write	Same as Real Mode
27	39		DOS Program Terminate, Stay Resident	Same as Real Mode

Table 2-4 V7875 Interrupt Vector Table

Interrupt No				
HEX.	DEX	IRQ Line	Real Mode	Protected Mode
28	40		DOS Keyboard Idle Loop	Same as Real Mode
29	41		DOS CON Dev. Raw Output	Same as Real Mode
2A	42		DOS 3.x+ Network Comm	Same as Real Mode
2B	43		DOS Internal Use	Same as Real Mode
2C	44		DOS Internal Use	Same as Real Mode
2D	45		DOS Internal Use	Same as Real Mode
2E	46		DOS Internal Use	Same as Real Mode
2F	47		DOS Print Spooler Driver	Same as Real Mode
30-60	48-96		Reserved by DOS	Same as Real Mode
61-66	97-102		User Available	Same as Real Mode
67-6F	103-111		Reserved by DOS	Same as Real Mode
70	112	IRQ8	Real Time Clock	
71	113	IRQ9	Redirect to IRQ2	
72	114	IRQ10	Not Assigned	
73	115	IRQ11	Not Assigned	
74	116	IRQ12	Mouse	
75	117	IRQ13	Math Coprocessor	
76	118	IRQ14	AT Hard Drive	
77	119	IRQ15	Flash Drive	
78-7F	120-127		Reserved by DOS	Same as Real Mode
80-F0	128-240		Reserved for BASIC	Same as Real Mode
F1-FF	241-255		Reserved by DOS	Same as Real Mode

2.5.2 PCI Interrupts

The Tsi148 VME Bridge and the PMC site of the V7875 connect Standard PCI Interrupt Lines to the PCI-E to PCI-X bridge. The PCI-E bridges (PLX PEX8114) convert the PCI INTx interrupts into virtual PCI Express INTA interrupts that are signaled back to the chipset over the PCI Express Interface.

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and de-assertion of an interrupt line, INTx#, is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device de-asserts its INTx# signal.

PCI defines one interrupt line for a single function device and up to four interrupt lines for a multifunction device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. **Figure 2-1** ***Interrupt Logic*** on page 49 depicts the V7875 interrupt logic pertaining to timer NVRAM operations and the PCI expansion site.

Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line, or each may have its own (up to a maximum of four functions), or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.

The slave PIC accepts the PCI interrupts through lines that are defined by the BIOS. The BIOS defines which interrupt line to utilize depending on which system requires the use of the line.

2.5.3 PCI Device Interrupt Map

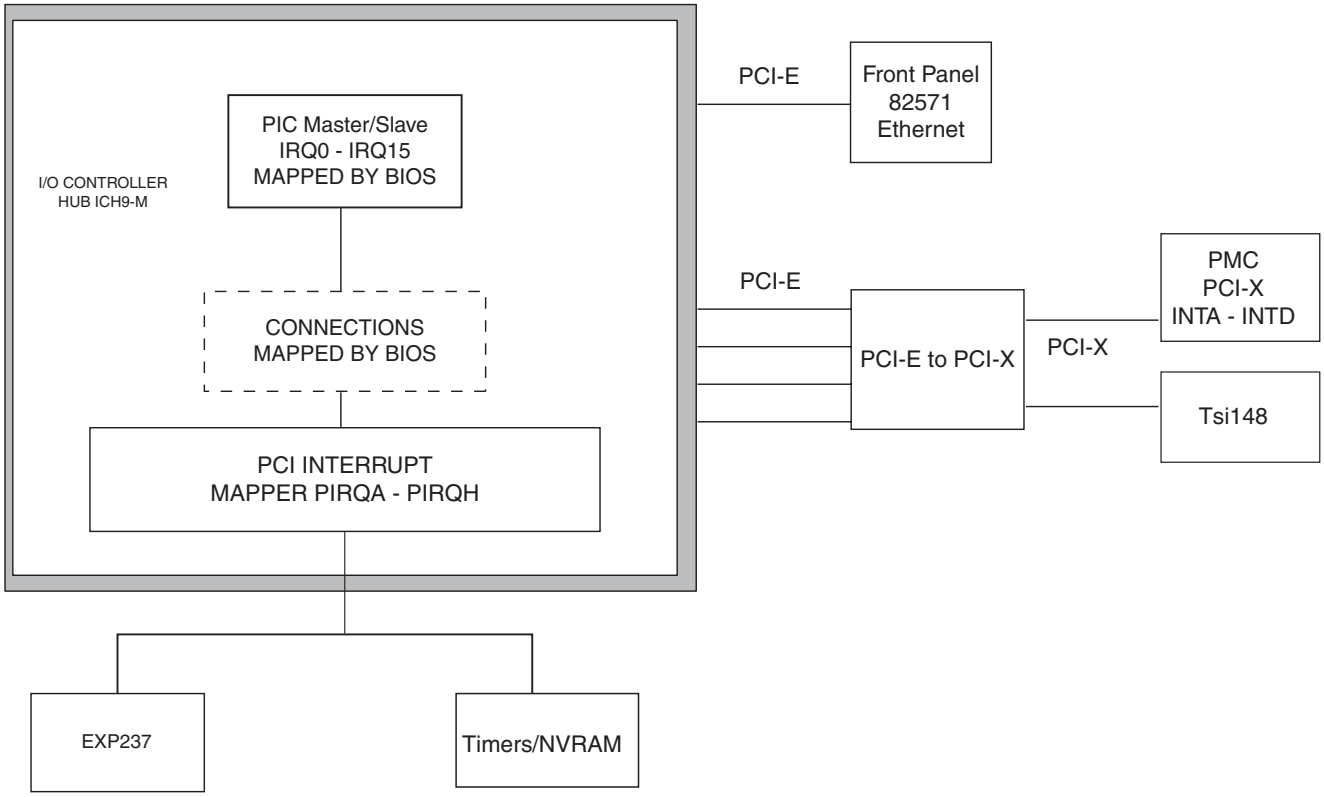
The PCI bus-based external devices include the PMC sites, Ethernet controller and the PCI-to-VME bridge. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the ICH2. This mapping is defined in Table 2-5.

The device PCI interrupt lines (INTA through INTD) that are present on each device cannot be modified.

Table 2-5 V7875 PCI Device Interrupt Mapping by the BIOS

Device	Component	Vendor ID	Device ID	CPU Address Map ID Select	PCI IRQ	Arbitration Request Line
PCI-to-VME Bridge	Tundra Tsi148	0x10E3	0x0148	AD16	INTA	REQ0
PMC	N/A	N/A	N/A	AD16	INTA	REQ0
Ethernet Controller	Intel 82571	0x8086	0x105E/ 0X1060	N/A	N/A	N/A
PCI Host Bridge	GMCH	0x8086	0x27A0	N/A	N/A	N/A
VGA Controller	GMCH	0x8086	0x27A2	N/A	N/A	N/A
Integrated Graphics	GMCH	0x8086	0x27A6	N/A	N/A	N/A
PCI-LPC Bridge	ICH9-M	0x8086	0x27B0	N/A	N/A	N/A
USB UHCI Controller	ICH9-M	0x8086	0x27C8 0x27C9 0x27CA 0x27CB	N/A	N/A	N/A
USB EHCI	ICH9-M	0x8086	0x27CC	N/A	N/A	N/A
SMBus Controller	ICH9-M	0x8086	0x27DA	N/A	N/A	N/A
PCI-E Controller	ICH9-M	0x8086	0x27D0	N/A	N/A	N/A
PCI-E Controller	ICH9-M	0x8086	0x27E0	N/A	N/A	N/A
DMI-PCI Bridge	ICH9-M	0x8086	0x2448	N/A	N/A	N/A
Integrated Ethernet	ICH9-M	0x8086	0x10F5	N/A	N/A	N/A
PCI-E Switch	PLX 8648	0x10B5	0x8648	N/A	N/A	N/A
PCI-E to PCI-X Bridge	Intel 41210	0x8086	0340&0341	N/A	N/A	N/A
Ethernet Controller	Intel 82573	0x8086	0x108B	N/A	N/A	N/A

Figure 2-1 Interrupt Logic



2.6 Integrated Peripherals

The V7875 incorporates the Windbond Super I/O (SIO) chip. The SIO provides the V7875 with two 16550 UART-compatible serial ports. The serial port signals for COM1 are available from the front panel, and the signals for COM2 are available through the rear I/O.

The SATA interface is provided by the Intel I/O Controller Hub (ICH9-M) chip. The SATA interface supports up to four channels. One SATA channel is routed to the optional CompactFlash socket. Two SATA channels are routed out the VME backplane and can be accessed using a ACC-0602RC*/ACC-0603RC RTM which terminates into standard SATA connectors. A fourth SATA channel is routed to the optional 0491 PMC Filler Module and is available via the panel's eSATA connector.

NOTE

Only an eSATA cable can be inserted into the optional 0491 PMC Filler Module . See **Figure 1-9, *Front Panel Layout/LED Status (Optional)*,** on page 35.

2.7 Dual 10/100/1000 Ethernet via the Front Panel

The V7875 supports Ethernet LANs with two Intel Ethernet controllers (a controller built into the ICH9M and a 82573 controller). 10Base-T, 100Base-TX and GbE options are supported via two front panel RJ45 connectors.

10Base-T A network based on the 10Base-T standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ45 connector is used with the 10Base-T standard. 10Base-T has a maximum length of 100 meters.

100Base-TX The V7875 also supports the 100Base-TX Ethernet. A network based on a 100Base-TX standard uses unshielded twisted-pair cables and an RJ45 connector. 100Base-TX has a maximum length of 100 meters.

1000Base-T The V7875 supports GbE offering speeds of 1000Mb/s. It is fully compatible with existing Ethernets, as it uses the same CSMA/CD and MAC protocols. 1000Base-T has a maximum length of 3000 meters using Single-mode Fiber-Optic cables.

2.7.1 Boot ROM BIOS

The V7875 supports booting on the front panel GbE ports using a ROM Ethernet BIOS. Refer to Section **3.15** ***Remote Ethernet Booting*** on page 62.

2.7.2 Rear Optional VITA 41.3 Ethernet Controller

The optional VITA 41.3 SERDES network capability is provided by the Intel 82571EB Dual Ethernet Controller for Gigabit Ethernet. The Ethernet controller is PCIe bus based and is software configurable. This SERDES based network capability provides 1000Base-T Ethernet and is provided by the P0 connector. (See **Table A-2 on page 68**.)

When the 0491 PMC Filler Module is installed, the rear Ethernet ports can be alternately directed to the front panel connectors on the module, thereby providing a total of four Gigabit Ethernet connectors on the front panel.

2.8 Video Graphics Adaptor

The V7875 supports high-resolution graphics and multimedia-quality video using the Intel GM45 Graphic Memory Controller Hub (GMCH) chipset internal graphics controller. Screen resolutions up to 1,600 x 1,200 colors (single view mode) are supported by the graphics adapter.

2.8.1 VGA Interface

The VGA interface can be accessed using an included adapter to adapt from the DVI-I front panel connector to a HD15 VGA connector. Supported display modes for VGA include:

Table 2-6 Partial List of Display Modes Supported for Analog

	Bits Per Pixel (Frequency) in Hz	
Resolution	16-bit	32-bit
640 x 480*		
800 x 600	60, 72, 75, 85, 100, 120	60, 72, 75, 85, 100, 120
1,024 x 768	60, 70, 75, 85, 100, 120	60, 70, 75, 85, 100, 120
1,152 x 864	60, 75, 85, 100	60, 75, 85, 100
1,280 x 600	60	60
1,280 x 720	60, 75, 85, 100	60, 75, 85, 100
1,280 x 768	60, 75, 85,	60, 75, 85
1,280 x 960	60, 75, 85	60, 75, 85
1,280 x 1,024	60, 75, 85, 100, 120	60, 75, 85, 100, 120
1,280 x 1,050	60, 75, 85	60, 75, 85
1,600 x 900	60, 75, 85, 100, 120	60, 75, 85, 100, 120
1,600 x 1,200	60, 75, 85, 100	60, 75, 85, 100
1680 x 1,050	60	60
1792 x 1344	60, 75	60, 75
1856 x 1392	60, 75	60, 75
1920 x 1080	60, 75, 85	60, 75, 85
1920 x 1200	60, 75	60, 75
1920 x 1440	60	60
2048 x 1536	60	60

*The Intel Extreme Graphics driver 14.36.3.4990 does not load at 640x480 resolution as set by BIOS. Default color depth = 4 with no frequency options.

2.8.2 Digital Visual Interface (DVI-I)

The V7875 supports a Digital Visual Interface that provides a high-speed digital connection for visual data types that are display technology independent. DVI-I is a display interface developed in response to the proliferation of digital flat-panel displays.

Table 2-7 Partial List of Display Modes Supported for Digital

	Bits Per Pixel (Frequency) in Hz	
Resolution	16-bit	32-bit
640 x 480*		
800 x 600	60	60
1024 x 768	60	60,

*The Intel Extreme Graphics driver 14.36.3.4990 does not load at 640x480 resolution as set by BIOS. Default color depth = 4 with no frequency options.

2.9 Universal Serial Bus

The V7875 provides four Universal Serial Bus (USB) connections on the front panel and four USB interface ports out the VME P2 connector. The onboard USB controller supports the standard USB interface Rev. 2.0.

NOTE

The use of USB to PS2 adapters is not supported.

2.10 Notes Regarding PCIe x16 I/O

As shown in the block diagram, the x16 PCIe port on the GMCH is used for various board I/O including the Gigabit Ethernet ports for the rear I/O (via P0) or the front (via the 0491 PMC Filler Module), the XMC site, and the board-to-board expansion connector. The PCIe bus on this port does not support the following transaction types:

- Inbound (upstream) memory writes with completion required
- Inbound (upstream) memory reads not mapped to main memory
- Inbound (upstream) memory reads which cross a 4k page boundary
- Inbound (upstream) I/O mapped transactions
- Inbound (upstream) Configuration mapped transactions
- Inbound (upstream) reserved or unsupported special cycles requiring completion
- Inbound (upstream) GTT aperture reads
- Inbound (upstream) memory reads or writes to Tile-Y DRAM space
- Peer-to-peer cycles.

The GMCH will terminate any unsupported transaction with an “Unsupported Request” error.

3 • Embedded PC/RTOS Features

GE's V7875 features additional capabilities beyond those of a typical desktop computer system. The units provide four software-controlled, general-purpose timers along with a programmable Watchdog Timer for synchronizing and controlling multiple events in embedded applications. The V7875 provides a bootable CompactFlash Disk system and 128 KByte of non-volatile RAM. Also, the V7875 supports an embedded intelligent VME bridge to allow compatibility with the most demanding VME applications. These features make the unit ideal for embedded applications, particularly where standard hard drives and floppy disk drives cannot be used.

3.1 VME Bridge

In addition to its PC/AT functions, the V7875 has the following VME features:

The Tundra Tsi148 allows VME to run at a bandwidth of up to 320 MByte/s along the full length of a 21-slot backplane. This increases the performance in the following ways:

- 2eSST VME transfers
- 8x faster than the 40 MByte/s transfer rate of VME64
- 3x faster than a multi-domain, 64-bit/66 MHz CompactPCI bus
- Broadcast Mode support for sending data to multiple cards at one time

Other standard features include:

- Legacy protocol support
- User-configured interrupter
- User-configured interrupt handler
- Full VME system controller functionality
- Two programmable DMA controllers
- System Controller auto detection

The V7875 VME interface is based on the high performance PCIX-to-VME interface from the Tundra Tsi148. Providing a 64-bit bus width capable of operating at 100 MHz, the Tundra Tsi148 uses PCI-X version 2.0 mode 1. Tsi148 is fully compliant with both 2eSST and VME64 Extension standards.

The functions and programming of the Tsi148-based VME interface are addressed in detail in the ***Tsi148 PCI/X-to-VME Bus Bridge User Manual***.

3.1.1 PCI-X To VME Bridge (Tsi148) Software Guidelines

Programmers writing code or using GE computer Board Support Packages (BSPs) for the Tsi148 Bridge as used on the V7875 single board computer, must be aware of requirements of the Tsi148-based PCI-X to VME architecture.

The V7875 PCI-X to VME Interface uses the Tundra Tsi148 2eSST Bridge. This architecture interfaces the VME to the onboard SBC PCI-X bus. In doing so, the user must be aware of the following guidelines as related to Software programming of the Tsi148:

Shared V7875 Memory: Any V7875 DRAM memory made available to another VME master through the Tsi148 is subject to dead lock that may cause a VME bus error unless specific precautions are taken. If onboard DRAM memory is slaved to the VME, and a program on the V7875 with slaved memory attempts to write (from the processor) to the VME through the Tsi148, then the user must first request ownership of the VME through the Device Wants Bus (DWB) Bit in the Tsi148, and be granted the VME, prior to doing writes to the Tsi148.

NOTE

Please see the Tsi148 Manual and Errata regarding the requirements to use the DWB bit of the Tsi148.

The user may also implement other methods of gaining ownership of the VME, such as Tsi148 semaphores. But, regardless of the method used, when using shared memory, the user must gain exclusive VME ownership prior to generating asynchronous VME writes.

Extremely Long VME Slave Response Time: VME slave devices (or VME BERR conditions) that have a DTAK (or BERR) response time of greater than 16µ can cause Bridge Ordering rule issues with intermixed reads and writes through the Tsi148. If the SBC user wishes to do an extended number (larger than the depth of the Tsi148 write post buffer) of consecutive writes from the processor to the VME through the Tsi148, and those writes can be intermixed with reads from another task, then the user must verify that all slaves within the system have DTACK response time of less than 16µ , and that the VME BERR timer of the system is set to 16µ max. Also, it is suggested that prior to doing any large VME transfer, the users should first request ownership of the VME through the DWB Bit in the Tsi148, and be granted the VME, prior to doing writes to the Tsi148.

NOTE

Please see the Tsi148 Manual and Errata regarding the requirements to use the DWB bit of the Tsi148.

The user may also implement other methods of gaining ownership of the VME, such as Tsi148 semaphores. But, regardless of the method used, when generating an extended number of consecutive processor to VME writes (larger than the depth of the Tsi148 write post buffer), the user must gain exclusive VME ownership prior to generating these asynchronous VME writes.

NOTE

Failure to implement the procedures outlined above may cause some system implementations to lockup or generate unwanted VME errors.

3.2 Embedded Functions

The V7875 provides non-volatile RAM (NVRAM), timers and a Watchdog Timer. These functions are required for embedded and real time applications. These embedded functions are located at base I/O address 0x600 (TIMER_WD_BASE_ADDRESS). This area contains control/status registers for timers, NVRAM access registers, and the board ID. The following table shows the Embedded Functions space.

Table 3-1 Embedded Functions Space Register

31 24	15 0			Register Offset
NVRAM Address		Reserved	Timer Enable Register	00h
TCSR4	TCSR3	TCSR2	TCSR1	04h
Timer 2		Timer 1		08h
Timer 3				0Ch
Timer 4				10h
NVRAM Read/Write Data				14h
Timer 4 IRQ Clear	Timer 3 IRQ Clear	Timer 2 IRQ Clear	Timer 1 IRQ Clear	18h
Feature Set 0007		Device Model 7875		1Ch

NOTE

All of the timers use interrupt 6 via the SERIRQ interface on the ICH9.

3.3 Timers

3.3.1 General

The V7875 provides four user-programmable timers (two 16-bit and two 32-bit) that are completely dedicated to user applications and are not required for any standard system function. Each timer is clocked by independent generators with selectable rates of 2 MHz, 1 MHz, 500 KHz and 250 KHz. Each timer may be independently enabled and each is capable of generating a system interrupt on timeout.

Events can be timed by either polling the timers or enabling the interrupt capability of the timer. A status register allows for application software to determine which timer is the cause of any interrupt.

3.3.2 Timer Enable Register

The timers are enabled via the Timer Enable Register located at offset 0x00 from base I/O address 0x600. The mapping of the bits in this register are as follows:

Table 3-2 TCSR1 Bit Mapping

Field	Bits	Read or Write	Description
Timer 1 Enable	TE[0]	R/W	0=disable, 1=enable
Timer 2 Enable	TE[1]	R/W	0=disable, 1=enable
Timer 3 Enable	TE[2]	R/W	0=disable, 1=enable
Timer 4 Enable	TE[3]	R/W	0=disable, 1=enable
Read Latch Select	TE[4]	R/W	0=latch individual timers, 1=latch all timers
Reserved	TE [7 ..5]	R/W	

All of these bits default to "0" after system reset.

Each timer can be independently enabled by writing a "1" to the appropriate "Timer x Enable" field.

The "Read Latch Select" bit is used to select the latching mode of the programmable timers. If this bit is set to "0", then each timer output is latched upon a read of the timer's LSB. For example, a read to the LSB of the TMRCCR2 register (Timer Current Count Register), address 0x0A, latches the count of timer 2. This continues for every read to any one of these registers. By setting this bit to "1", all four timer outputs will be latched only on a read to TMRCCR1's LSB, address 0x08. Therefore, to capture the current count of all four timers at the same time, perform a read to the TMRCCR1 first, followed by a read to TMRCCR2, TMRCCR3 and TMRCCR4. The first read causes all four timer values to be latched at the same time. The subsequent reads to the other timer registers do not latch new count values and may be read in any order.

3.3.3 Timer Control Status Register (TCSR)

Each timer is controlled and monitored via the Timer Control Status Register TCSRx, located at the following addresses:

Table 3-3 Time Control Status Registers

Timer	Address
TCSR1	0x04
TCSR2	0x05
TCSR3	0x06
TCSR4	0x07

The mapping of the bits in the registers is as follows:

Table 3-4 Timer Control Status Register Bit Map

Field	Bits	Read or Write	Description
IRQ Enable	TCSR[0]	R/W	0=disable, 1=enable
Timer Clock Select	TCSR[2. .1]	R/W	See Table 3-5 "Timer x Clock Select"
Read Timer	TCSR[3]	R/W	0=current timer value 1=timer load value
Reserved	TCSR[6..4]	R/W	
Interrupt	TCSR[7}	R/W	0=normal, 1=generate interrupt
All of these bits default to "0" after system reset.			

The "IRQ Enable" bit must be set to a "1" for the timer to be able to generate an interrupt.

Each timer has an independently selectable clock source which is selected by the bit pattern in the "Timer x Clock Select" field as follows:

Table 3-5 Timer x Clock Select

Clock Rate	Bit 2	Bit 1
2 MHz	0	0
1 MHz	0	1
500 KHz	1	0
250 KHz	1	1

The "Read Timer" bit selects between reading the current timer value or reading the timer load value when the timer data is read. Setting this bit to "0" will enable the reading of the current timer value. Setting this bit to a "1" will enable the reading of the value that was loaded into the timer.

When the timer generates an interrupt, the "Interrupt" bit is read as a "1" and is cleared with a write to the appropriate "Timer x IRQ Clear" register. Alternately, writing a "0" to TCSR[7] will also clear the interrupt. When this bit is read as a "0", the timer has not created an interrupt. When a "1" is written into this bit, a single interrupt will be generated when the timer's "IRQ Enable" bit is enabled.

3.4 Timer 1 Value Register

Timer 1 is a 16 bit timer that is located at offset 0x08 from base I/O address 0x600. When this field is read, the value returned is either the current value or the loaded value, depending on the setting of TCSR1[3]. The current timer count value is latched when the offset address 0x08 is read.

3.5 Timer 2 Value Register

Timer 2 is a 16 bit timer that is located at offset 0x0A from base I/O address 0x600. When this field is read, the value returned is either the current count value or the loaded value, depending on the setting of TCSR2[3]. The current timer count value is latched when either the offset address 0x0A or the offset address 0x08 is read, depending on the setting of TER[4].

3.6 Timer 3 Value Register

Timer 3 is a 32 bit timer that is located at offset 0x0C from base I/O address 0x600. When this field is read, the value returned is either the current count value or the loaded value, depending on the setting of TCSR3[3]. The current timer count value is latched when either the offset address 0x0C or the offset address 0x08 is read depending on the setting of TER[4].

3.7 Timer 4 Value Register

Timer 4 is a 32 bit timer that is located at offset 0x10 from base I/O address 0x600. When this field is read, the value returned is either the current value or the loaded value, depending on the setting of TCSR4[3]). The current timer count value is latched when either the offset address 0x10 or the offset address 0x08 is read, depending on the setting of TER[4].

3.8 Timer 1 IRQ Clear (T1IC)

The Timer 1 IRQ Clear (T1IC) register is used to clear an interrupt caused by Timer 1. Writing to this register, located at offset 0x18 from base I/O address 0x600, causes the interrupt from Timer 1 to be cleared. This can also be done by writing a "0" to TCSR1[7]. The T1IC register is write only and the data written is irrelevant.

3.9 Timer 2 IRQ Clear (T2IC)

The Timer 2 IRQ Clear (T2IC) register is used to clear an interrupt caused by Timer 2. Writing to this register, located at offset 0x19 from base I/O address 0x600, causes the interrupt from Timer 2 to be cleared. This can also be done by writing a "0" to TCSR2[7]. The T2IC register is write only and the data written is irrelevant.

3.10 Timer 3 IRQ Clear (T3IC)

The Timer 3 IRQ Clear (T3IC) register is used to clear an interrupt caused by Timer 3. Writing to this register, located at offset 0x1A from base I/O address 0x600, causes the interrupt from Timer 3 to be cleared. This can also be done by writing a "0" to TCSR3[7]. The T3IC register is write only and the data written is irrelevant.

3.11 Timer 4 IRQ Clear (T4IC)

The Timer 4 IRQ Clear (T4IC) register is used to clear an interrupt caused by Timer 4. Writing to this register, located at offset 0x1B from base I/O address 0x600, causes the interrupt from Timer 4 to be cleared. This can also be done by writing a "0" to TCSR4[7]. The T3IC register is write only and the data written is irrelevant.

3.12 Watchdog Timer

A Watchdog timer is provided using the ICH9 TCO timer. Refer to Intel documentation for proper usage.

3.13 NVRAM

The V7875 provides 128 KByte of non-volatile SRAM. The contents of this memory are retained when the power to the board is removed. The NVRAM is accessed using an index register set. The NVRAM address register is found at offset 00h. The NVRAM Read/Write Data register is found at offset 14h.

3.14 CompactFlash Disk

The V7875 features an optional onboard CompactFlash mass storage system with a capacity of up to 8 GByte. This CompactFlash Disk appears to the user as an intelligent ATA (IDE) disk drive with the same functionality and capabilities as a “rotating media” IDE hard drive. The V7875 BIOS includes an option to allow the board to boot from the CompactFlash with user-provided operating system.

3.15 Remote Ethernet Booting

The V7875 is capable of booting from a server using Gigabit Ethernet over a network utilizing the Boot ROM BIOS. The BIOS gives you the ability to remotely boot the V7875 using a PXE network protocol. The Ethernet may be connected through the front panel RJ45 connectors, or the optional P0 connector to boot remotely. This feature allows users to create systems without the worry of disk drive reliability or the extra cost of adding CompactFlash drives.

3.15.1 Boot BIOS Features

- PXE boot support
- Detailed boot configuration screens
- Optional disabling of local boots
- Dual-boot option lets users select network or local booting

Maintenance

If a GE product malfunctions, please verify the following:

1. Software version resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact GE for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return from Customer Care.**

GE Customer Care is available at: 1-800-433-2682 in North America, or +1-780-401-7700 for international calls. Or, visit our website **www.ge-ip.com.**

The V7875 is factory populated with an Intel Core 2 Duo processor.

To change the memory size or CompactFlash size, contact Customer Care to receive a Return Material Authorization (RMA).

Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

A • Appendix A: Connectors and Pinouts

A.1 VME P1/P2 Pinout

The V7875 has several connectors for its I/O ports. Wherever possible, the V7875 uses connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a variety of systems.

Figure A-1 V7875 Connector Location Top Assembly

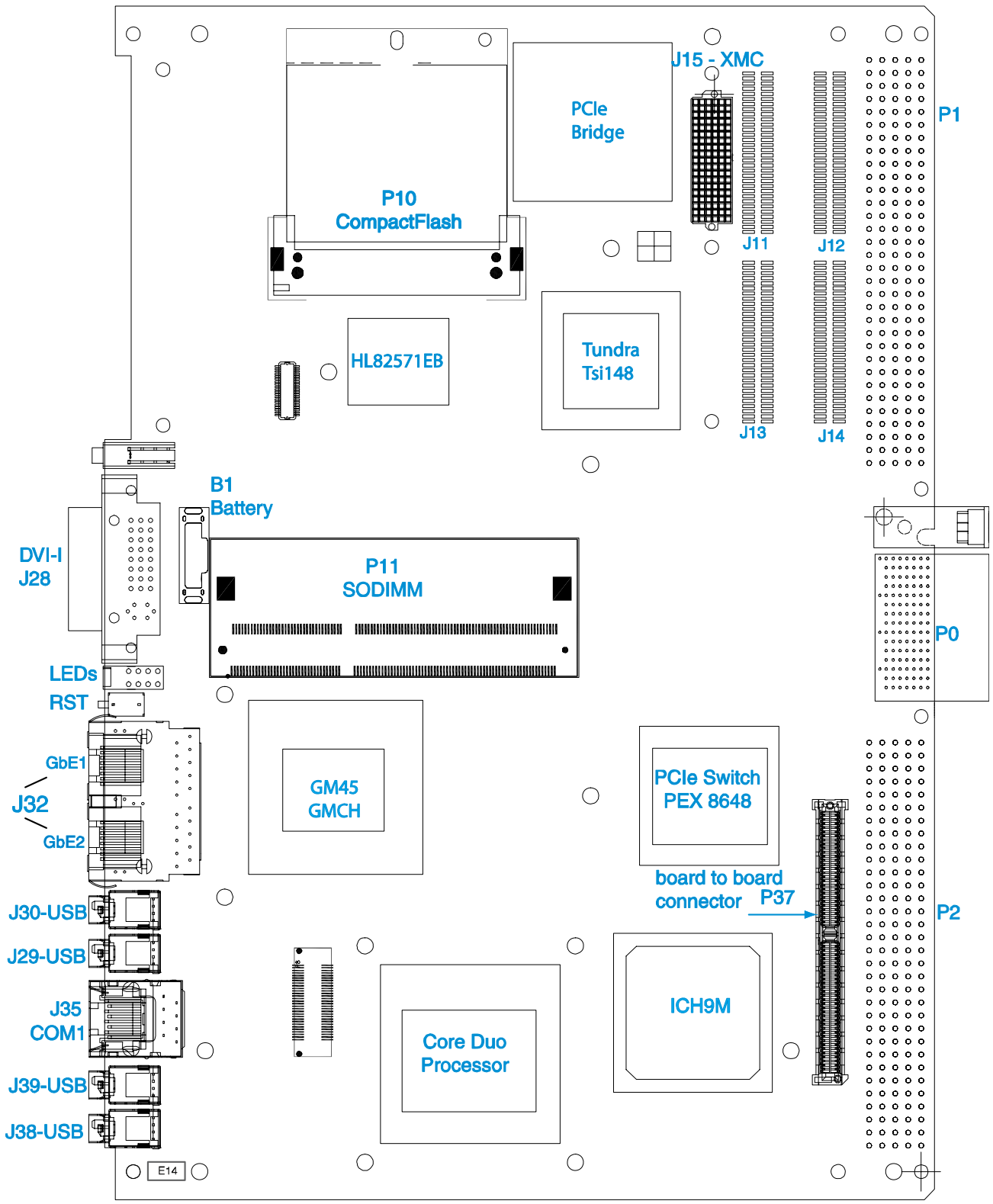
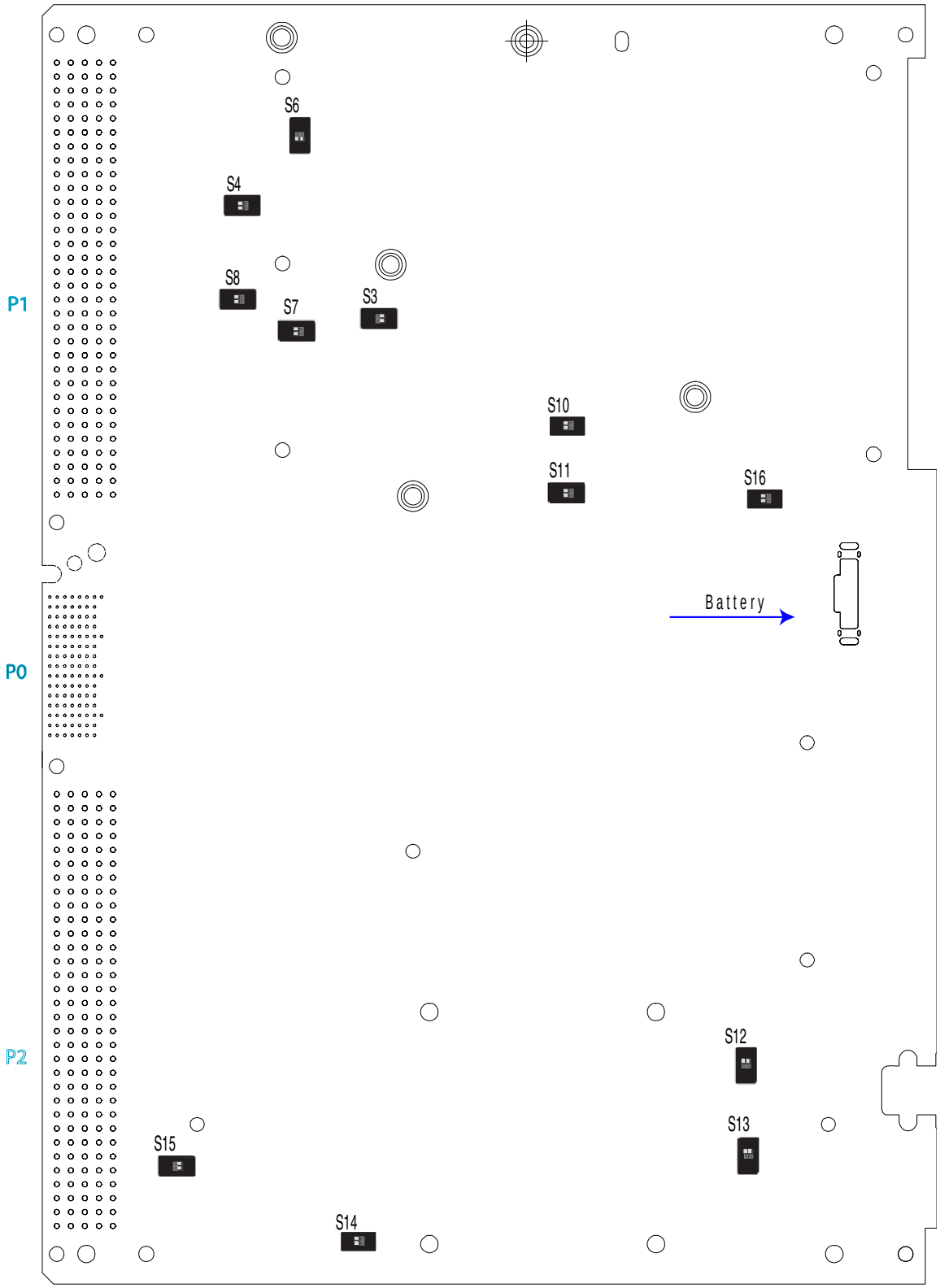


Figure A-2 V7875 Switch Location Bottom Assembly



A.2 VME Connector Pinout (P1 and P2)

Figure A-3 VME Connectors

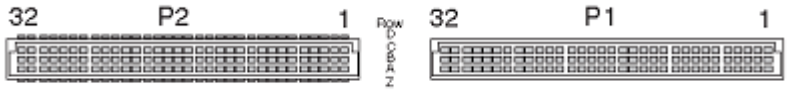


Table A-1 VME P1 and P2 Pinout

Pin#	P1 Row A Signal	P1 Row B Signal	P1 Row C Signal	P2 Row Z Signal	P2 Row A Signal	P2 Row B Signal	P2 Row C Signal	P2 Row D Signal
1	D00	BBSY#	D08	CONN [2]	GND	VCC_5.0	SP1_TX	CONN [1]
2	D01	BCLR#	D09	GND	USB_P5N	GND	NC	CONN [3]
3	D02	ACFAIL	D10	CONN [5]	USB_P5P	RETRY#	NC	CONN [4]
4	D03	BG0IN#	D11	GND	USB_OC5#	A24	SP1_RX	CONN [6]
5	D04	BG0OUT#	D12	CONN [8]	GND	A25	NC	CONN [7]
6	D05	BG1IN#	D13	GND	USB_P4N	A26	NC	CONN [9]
7	D06	BG1OUT#	D14	CONN [11]	USB_P4P	A27	NC	CONN [10]
8	D07	BG2IN#	D15	GND	USB_OC4#	A28	NC	CONN [12]
9	GND	BG2OUT#	GND	CONN [14]	GND	A29	RTM_CONF_GP	CONN [13]
10	SYSCLK	BG3IN#	SYSFAIL#	GND	USB_P3P	A30	VCC_5.0	CONN [15]
11	GND	BG3OUT#	BERR#	CONN [17]	USB_P3N	A31	VCC_-12 V	CONN [16]
12	DS1#	BR0#	SYSRST#	GND	USB_OC3#	GND	GND	CONN [18]
13	DS0#	BR1#	LWORD#	CONN [20]	GND	VCC_5.0	SATA1_RXN	CONN [19]
14	WRITE#	BR2#	AM5	GND	USB_P2N	D16	SATA1_RXP	CONN [21]
15	GND	BR3#	A23	CONN [23]	USB_P2P	D17	GND	CONN [22]
16	DTACK#	AM0	A22	GND	USB_OC2#	D18	SATA1_TXN	CONN [24]
17	GND	AM1	A21	CONN [26]	GND	D19	SATA1_TXP	CONN [25]
18	AS#	AM2	A20	GND	VCC_5.0	D20	GND	CONN [27]
19	GND	AM3	A19	CONN [29]	VCC_12.0	D21	GND	CONN [28]
20	IACK#	GND	A18	GND	GND	D22	SATA2_RXN	CONN [30]
21	IACKIN#	N/C	A17	CONN [32]	NC	D23	SATA2_RXP	CONN [31]
22	IACKOUT#	N/C	A16	GND	NC	GND	GND	CONN [33]
23	AM4	GND	A15	CONN [35]	GND	D24	SATA2_TXN	CONN [34]
24	A07	IRQ7	A14	GND	NC	D25	SATA2_TXP	CONN [36]
25	A06	IRQ6	A13	CONN [38]	NC	D26	GND	CONN [37]
26	A05	IRQ5	A12	GND	GND	D27	GND	CONN [39]
27	A04	IRQ4	A11	CONN [41]	NC	D28	GND	CONN [40]
28	A03	IRQ3	A10	GND	NC	D29	GND	CONN [42]
29	A02	IRQ2	A09	CONN [44]	GND	D30	NC	CONN [43]
30	A01	IRQ1	A08	GND	NC	D31	NC	CONN [45]
31	VCC_-12 V	N/C	VCC_12.0	CONN [46]	NC	GND	NC	GND
32	VCC_5.0	VCC_5.0	VCC_5.0	GND	GND	VCC_5.0	Reserved VME_Standby_ 3.3	VCC_5.0

A.3 Optional Vita 41.3 Connector (P0)

Figure A-4 Optional VITA 41.3 Connector

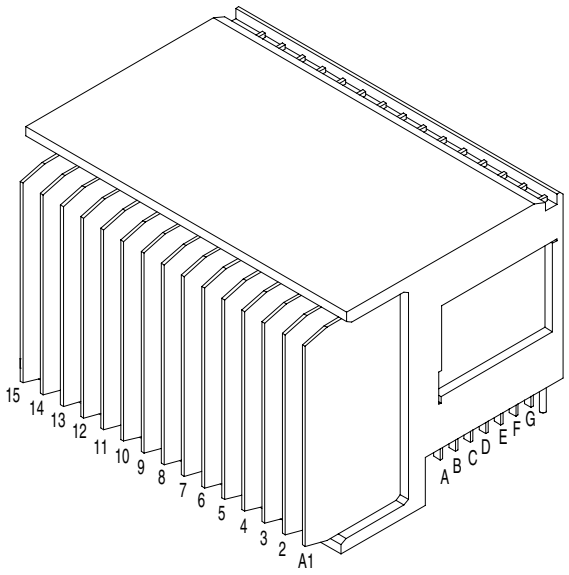


Table A-2 Optional Vita 1.3 Connector (P0)

Optional Vita 41.3 Connector (P0)							
Pin #	Row A	Row B	Row C	Row D	Row E	Row F	Row G
1	SERDES_RX_A[1]	SERDES_RX_A[2]	GND	SERDES_TX_A[1]	SERDES_TX_A[2]	GND	N/C
2	GND	N/C	N/C	GND	N/C	N/C	GND
3	N/C	N/C	GND	N/C	N/C	GND	N/C
4	GND	N/C	N/C	GND	N/C	N/C	GND
5	N/C	N/C	GND	N/C	N/C	GND	N/C
6	GND	N/C	N/C	GND	N/C	N/C	GND
7	N/C	N/C	GND	N/C	N/C	GND	N/C
8	GND	N/C	N/C	GND	N/C	N/C	GND
9	N/C	N/C	GND	N/C	N/C	GND	N/C
10	GND	N/C	N/C	GND	N/C	N/C	GND
11	N/C	N/C	GND	N/C	N/C	GND	N/C
12	GND	SERDES_RX_B[1]	SERDES_RX_B[2]	GND	SERDES_TX_B[1]	SERDES_TX_B[2]	GND
13	N/C	N/C	GND	N/C	N/C	GND	N/C
14	GND	N/C	N/C	GND	N/C	N/C	GND
15	N/C	N/C	GND	N/C	N/C	GND	N/C

A.4 Serial Connector RJ45 (J35)

COM 1 Serial Port Connector is a standard RJ45 connector as shown in the figure and table below:

Figure A-5 Serial Connector (J35)

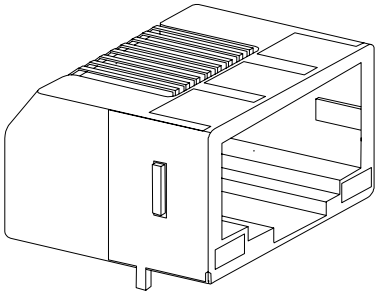


Table A-3 Serial Connector Pinout (J35)

Pin	RS232 Signal	RS422 Signal
1	DCD	RXD-
2	RTS	RTS+
3	GND	TXD
4	TXD	TXD
5	RXD	RXD
6	GND	GND
7	CTS	CTS
8	DTR	DTR

NOTE: See the appropriate table of jumper and switch settings for configuring.

A.5 USB Connectors and Pinout (J38 and J39)

The two USB ports are industry standard 4-position shielded connectors. The figure below depicts a representation of the connectors, and table that follows shows the pinout (same for each).

Figure A-6 USB Port

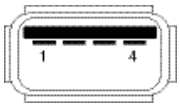


Table A-4 USB Connectors (J38/J39)

Pin	Signal	Function
1	USB_VCC	USB Power
2	USB-	USB Data -
3	USB+	USB Data +
4	USBG	USB Ground

A.6 DVI-I Connector and Pinout (J28)

The DVI-I port on the V7875 is controlled by the Intel GM45 Graphic and Memory Controller Hub (GMCH). The GMCH is hardware and BIOS compatible with the industry SVGA and digital video standards supporting both VESA high-resolution and extended video modes.

Figure A-7 DVI-I Connector and Pinout (J28)

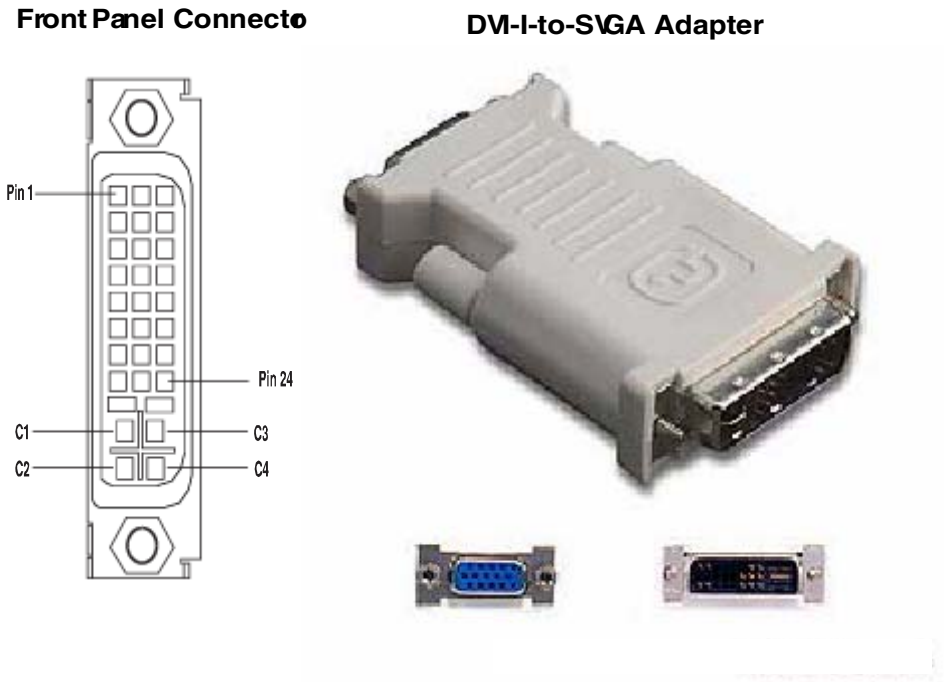


Table A-5 DVI-I Connector Pinout

Pin#	Signal Assignment	Pin#	Signal Assignment	Pin#	Signal Assignment
1	Data 2-	9	Data 1-	17	Data 0-
2	Data 2+	10	Data 1+	18	Data 0+
3	GND	11	GND	19	GND
4	N/C	12	N/C	20	N/C
5	N/C	13	N/C	21	N/C
6	DDC Clock	14	+5VDC Power (750 mA)	22	GND
7	DDC Data	15	GND (Return for +5, HSync and VSync)	23	Clock+
8	Analog VSync	16	Hot Plug Detect	24	Clock-
C1	Analog Red	C2	Analog Green	C3	Analog Blue
C4	Analog HSync	C5	Analog GND (RGB return)		

A.7 Gigabit Ethernet Connector and Pinout (J32)

The pinout diagram for the Gigabit Ethernet connector and pinout are shown in the following figure and table:

Figure A-8 GbE Connector

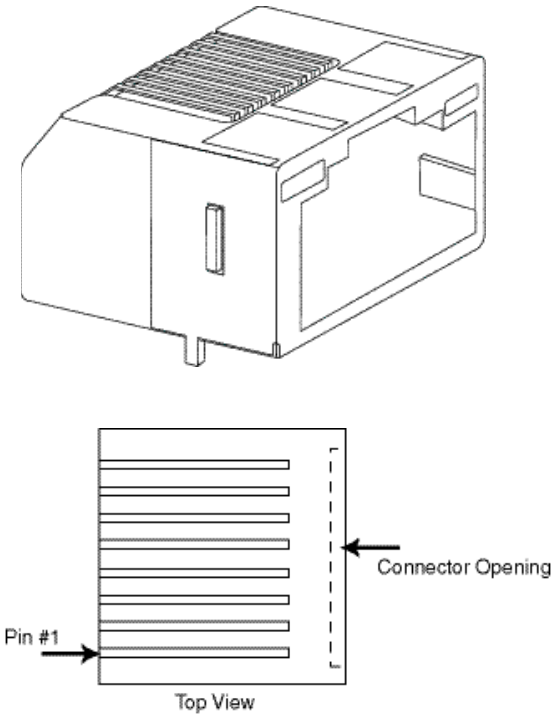


Table A-6 Ethernet Connectors 10/100/1000 Mbit (J32)

Pin	Signal	Function
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	TX_CT_OUT	Transmit Center Tap Out
5	TX_CT_OUT	Transmit Center Tap Out
6	RD-	Receive Data
7	RX_CT_OUT	Receive Center Tap Out
8	RX_CT_OUT	Receive Center Tap Out

A.8 PMC Connector and Pinouts

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. **Table A-7** through **Table A-11** are the pinouts for the XMC/PMC connectors (J11, J12, J13 and J14).

A.8.1 PMC Connectors and Pinouts (J11)

Figure A-9 PMC Connector and Pinout (J11)

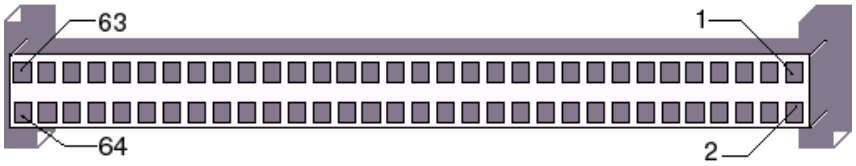


Table A-7 PMC Connector Pinout (J11)

PMC Connector (J11)				PMC Connector (J11)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	JTAG.TCK	2	-12	33	FRAME#	34	GND
3	GND	4	INTA3	35	GND	36	IRDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	+5 V
7	BMODE1	8	+5 V	39	PCIXCAP	40	LOCK#
9	INTD#	10	NC	41	SDONE#	42	+3.3V
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	+3.3V	46	AD[15]
15	GND	16	GNT#	47	AD[12]	48	AD[11]
17	REQ#	18	+5 V	49	AD[9]	50	+5 V
19	+3.3V	20	AD[31]	51	GND	52	C/BE[0]#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE[3]#	57	+3.3V	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5 V	61	AD[0]	62	+5 V
31	+3.3V	32	AD[17]	63	GND	64	REQ64#

A.8.2 PMC Connector and Pinouts (J12)

Figure A-10 Connector and Pinout (J12)

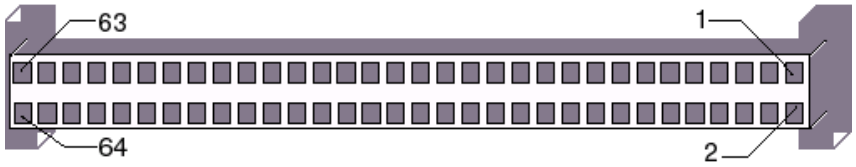


Table A-8 PMC Connector Pinout (J12)

PMC Connector (J12)				PMC Connector (J12)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12 V	2	JTAG_TRST	33	GND	34	NC
3	JTAG_TMS_2	4	JTAG_TDO	35	TRDY#	36	+3.3V
5	JTAG_TDI	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3V	42	SERR#
11	+3.3V	12	+3.3V	43	C/BE[1]#	44	GND
13	RST#	14	GND	45	AD[14]	46	AD[13]
15	+3.3V	16	GND	47	M66EN	48	AD[10]
17	PME#	18	GND	49	AD[8]	50	+3.3V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3V	54	NC
23	AD[24]	24	+3.3V	55	NC	56	GND
25	IDSEL	26	AD[23]	57	NC	58	NC
27	+3.3V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	ACK64#	62	+3.3V
31	AD[16]	32	C/BE[2]#	63	GND	64	NC

A.8.3 PMC Connector and Pinout (J13)

Figure A-11 Connector and Pinout (J13)

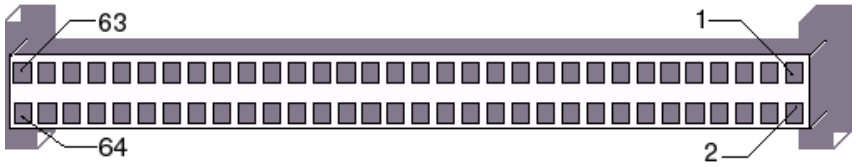


Table A-9 PMC Connector and Pinout (J13)

PMC Connector (J13)				PMC Connector (J13)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	NC	2	GND	33	GND	34	AD[48]
3	GND	4	CBE[7]#	35	AD[47]	36	AD[46]
5	CBE[6]#	6	CBE[5]	37	AD[45]	38	GND
7	CBE[4]#	8	GND	39	+3.3V	40	AD[44]
9	+3.3V	10	PAR64	41	AD[43]	42	AD[42]
11	AD[63]	12	AD[62]	43	AD[41]	44	GND
13	AD[61]	14	GND	45	GND	46	AD[40]
15	GND	16	AD[60]	47	AD[39]	48	AD[38]
17	AD[59]	18	AD[58]	49	AD[37]	50	GND
19	AD[57]	20	GND	51	GND	52	AD[36]
21	+3.3V	22	AD[56]	53	AD[35]	54	AD[34]
23	AD[55]	24	AD[54]	55	AD[33]	56	GND
25	AD[53]	26	GND	57	+3.3V	58	AD[32]
27	GND	28	AD[52]	59	NC	60	NC
29	AD[51]	30	AD[50]	61	NC	62	GND
31	AD[49]	32	GND	63	GND	64	NC

A.8.4 PMC Connector and Pinout (J14)

Figure A-12 Connector and Pinout (J14)

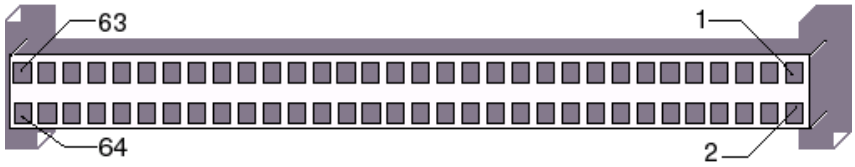


Table A-10 PMC Connector and Pinout (J14)

PMC Connector (J14)						PMC Connector (J14)					
Left Side			Right Side			Left Side			Right Side		
Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To	Pin	Name	Connected To
1	CONN[1]	P2 pin D1	2	CONN[2]	P2 pin Z1	33	CONN[33]	P2 pin D22	34	CONN[34]	P2 pin D23
3	CONN[3]	P2 pin D2	4	CONN[4]	P2 pin D3	35	CONN[35]	P2 pin Z23	36	CONN[36]	P2 pin D24
5	CONN[5]	P2 pin Z3	6	CONN[6]	P2 pin D4	37	CONN[37]	P2 pin D25	38	CONN[38]	P2 pin Z25
7	CONN[7]	P2 pin D5	8	CONN[8]	P2 pin Z5	39	CONN[39]	P2 pin D26	40	CONN[40]	P2 pin D27
9	CONN[9]	P2 pin D6	10	CONN[10]	P2 pin D7	41	CONN[41]	P2 pin Z27	42	CONN[42]	P2 pin D28
11	CONN[11]	P2 pin Z7	12	CONN[12]	P2 pin D8	43	CONN[43]	P2 pin D29	44	CONN[44]	P2 pin Z29
13	CONN[13]	P2 pin D9	14	CONN[14]	P2 pin Z9	45	CONN[45]	P2 pin D30	46	CONN[46]	P2 pin Z31
15	CONN[15]	P2 pin D10	16	CONN[16]	P2 pin D11	47	CONN[47]	NC	48	CONN[48]	NC
17	CONN[17]	P2 pin Z11	18	CONN[18]	P2 pin D12	49	CONN[49]	NC	50	CONN[50]	NC3
19	CONN[19]	P2 pin D13	20	CONN[20]	P2 pin Z13	51	CONN[51]	NC	52	CONN[52]	NC
21	CONN[21]	P2 pin D14	22	CONN[22]	P2 pin D15	53	CONN[53]	NC	54	CONN[54]	NC
23	CONN[23]	P2 pin Z15	24	CONN[24]	P2 pin D16	55	CONN[55]	NC	56	CONN[56]	NC
25	CONN[25]	P2 pin D17	26	CONN[26]	P2 pin Z17	57	CONN[57]	NC	58	CONN[58]	NC
27	CONN[27]	P2 pin D18	28	CONN[28]	P2 pin D19	59	CONN[59]	NC	60	CONN[60]	NC
29	CONN[29]	P2 pin Z19	30	CONN[30]	P2 pin D20	61	CONN[61]	NC	62	CONN[62]	NC
31	CONN[31]	P2 pin D21	32	CONN[32]	P2 pin Z21	63	CONN[63]	NC	64	CONN[64]	NC

A.9 XMC Connector and Pinout (J15)

Table A-11 XMC Connector and Pinout (J15)

Row A		Row B		Row C		Row D		Row E		Row F	
1	TX8+	1	TX8-	1	3.3V	1	TX9+	1	TX9-	1	5V
2	GND	2	GND	2	TRST#	2	GND	2	GND	2	RST#
3	TX10+	3	TX10-	3	3.3V	3	TX11+	3	TX11-	3	5V
4	GND	4	GND	4	TCK	4	GND	4	GND	4	MRSTO#
5	NC	5	NC	5	3.3V	5	NC	5	NC	5	5V
6	GND	6	GND	6	TMS	6	GND	6	GND	6	12V
7	NC	7	NC	7	3.3V	7	NC	7	NC	7	5V
8	GND	8	GND	8	TDI	8	GND	8	GND	8	-12V
9	NC	9	NC	9	NC	9	NC	9	NC	9	5V
10	GND	10	GND	10	TDO	10	GND	10	GND	10	GA0
11	RX8+	11	RX8-	11	MBIST#	11	RX9+	11	RX9-	11	5V
12	GND	12	GND	12	GA1	12	GND	12	GND	12	PRS#
13	RX10+	13	RX10-	13	3.3V	13	RX11+	13	RX11-	13	5V
14	GND	14	GND	14	GA2	14	GND	14	GND	14	MSDA
15	NC	15	NC	15	NC	15	NC	15	NC	15	5V
16	GND	16	GND	16	MVRMO	16	GND	16	GND	16	MSCL
17	NC	17	NC	17	RSVD	17	NC	17	NC	17	NC
18	GND	18	GND	18	NC	18	GND	18	GND	18	NC
19	CLK+	19	CLK-	19	NC	19	WAKE#	19	ROOT#	19	NC

A.9.1 Board to Board Connector (P37)

The Board to Board Connector, P37 is only for use with GE expansion products designed for the V7875. Please contact the GE sales representative for more information.

B • Appendix B: AMI BIOS Setup Utility

This appendix gives a brief description of the setup options in the system BIOS. Due to the custom nature of GE SBCs, your BIOS options may vary from the options discussed in this appendix.

To Access the First Boot setup screen, press the F11 key at the beginning of boot.

To access the setup screens, press the DEL key at the beginning of boot.

B.1 First Boot Menu

The V7875 has a First Boot menu enabling the user to, *on a one time basis*, select a drive device to boot from. This feature is useful when installing from a bootable disk. For example, when installing an operating system from a CD, enter the First Boot menu and use the arrows keys to highlight ATAPI CD-ROM Drive. Press ENTER to continue with system boot.

This feature is accessed by pressing the F11 key at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only, and will not be used during the next boot-up of the system.

If you have trouble accessing this feature, disable the QuickBoot Mode in the Main BIOS setup screen. Exit, saving changes and retry accessing the First Boot menu.

Table B-1 AMI BIOS First Boot Menu

Boot Menu
1. + Removable Devices
2. + Hard Drive
3. ATAPI CD-ROM Drive
4. MBA UNDI (Bus 1 Slot 6) LAN 1
<Enter Setup>

B.2 Main Menu

The Main BIOS setup menu screen has two main areas. The left frame displays all the options that can be configured. “Grayed-out” options cannot be configured. Options in blue can be configured. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white and a text message in the right frame gives a brief description of the option.

The Main menu reports the BIOS revision, processor type and clock speed, and allows the user to set the system’s clock and calendar. Use the left and right arrow keys to select other screens.

NOTE

Below is a sample of the Main screen. The information displayed on your screen will reflect your actual system.

Table B-2 AMI BIOS Main Menu

```
                              BIOS SETUP UTILITY
Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit

System Overview                                  Use [Enter], [TAB]
                                                 Or [SHIFT-TAB] to
AMIBIOS                                          Select a field.
Version : 08.00.10
Build Date : 03/02/04                            Use [+] or [-] to
ID  : V7875_16                                   Configure system
                                                 Time.
Processor
Type  : Intel(R) Pentium (R) M processor 1600MH
Speed  : 1600MHz

System Memory
Size  : 1016MB

System Time    [11:39:40]                        ←→  Select Screen
System Date    [Tue 03/04/2004]                  ↑↓  Select Item
                                                 +-  Change Field
                                                 Tab Select Field
                                                 F1  General Help
                                                 F10 Save and Exit
                                                 ESC Exit
```

002.53 (C) Copyright 1985-2002, American Megatrends, Inc.

B.3 Advanced BIOS Setup Menu

The Advanced BIOS Setup menu allows the user to configure some CPU settings, the IDE bus, SCSI devices and other external devices and internal drives.

Select the *Advanced* tab from the setup screen to enter the Advanced BIOS Setup screen. You can select the items in the left frame of the screen, such as Super I/O Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. A sample of the Advanced BIOS Setup screen is shown below.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to Section **1.4.1 *Clear CMOS/Password and BIOS Boot Mode*** on page 27 for instructions on clearing the CMOS.

Table B-3 AMI BIOS Advanced Menu

```
                              BIOS SETUP UTILITY
Main | Advanced | PCIPnP | Boot | Security | Chipset | Exit

Advanced Settings                                  Configure CPU.

WARNING: Setting wrong values in below sections
         may cause system to malfunction.

➢  CPU Configuration
➢  IDE Configuration
➢  Floppy Configuration
➢  SuperIO Configuration
➢  Remote Access Configuration
➢  USB Configuration

                                                   ←→   Select Screen
                                                   ↑↓   Select Item
                                                   Enter Go to Sub Screen
                                                   F1   General Help
                                                   F10  Save and Exit
                                                   ESC  Exit
```

002.53 (C) Copyright 1985-2002, American Megatrends, Inc.

Options shown may not be available on your system.

B.4 PCI/PnP Setup Menu

Included in this screen is the control of internal peripheral cards, as well as various interrupts. From this menu, the user can also determine if the system's plug-and-play is enabled or disabled.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to Section **1.4.1** ***Clear CMOS/Password and BIOS Boot Mode*** on page 27 for instructions on clearing the CMOS.

NOTE

Below is a sample screen of the PCI/PnP menu; options in your system may be different from those shown.

Table B-4 AMI BIOS PCI/PnP Menu

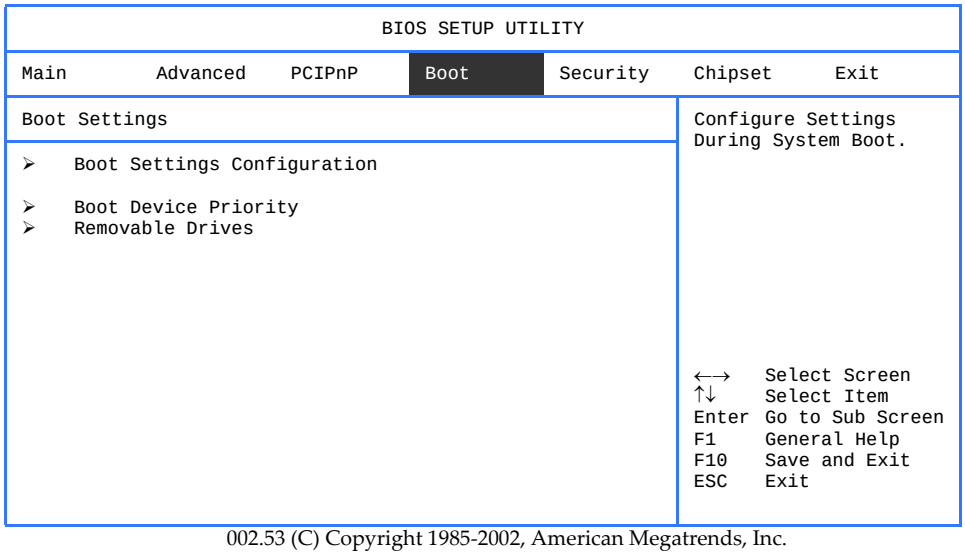
```
                              BIOS SETUP UTILITY
Main      Advanced   PCIPnP   Boot      Security   Chipset   Exit
Advanced PCI/PnP Settings                          NO: lets the BIOS
                                                   configure all the
WARNING: Setting wrong values in below sections    devices in the system.
         may cause system to malfunction.          YES: lets the
                                                   operating system
Plug & Play O/S                        [Yes]       configure Plug and
PCI Latency Timer                      [64]        Play (PnP) devices not
Allocate IRQ to PCI VGA                [Yes]       required for boot if
Palette Snooping                       [Disabled]  your system has a Plug
PCI IDE BusMaster                      [Disabled]  and Play operating
OffBoard PCI/ISA IDE Card              [Auto]      system.


IRQ3                                   [Available]
IRQ4                                   [Available]
IRQ5                                   [Available]  ←→  Select Screen
IRQ7                                   [Available]  ↑↓  Select Item
IRQ9                                   [Available]  +-  Change Option
IRQ10                                  [Available]  F1  General Help
IRQ11                                  [Available]  F10 Save and Exit
IRQ14                                  [Available]  ESC Exit
```

002.53 (C) Copyright 1985-2002, American Megatrends, Inc.

B.5 Boot Setup Menu

Use the Boot Setup menu to set the priority of the boot devices, including booting from a remote network. The devices shown in this menu are the bootable devices detected during POST. If a drive is installed that does not appear, verify the hardware installation. Also available in this screen are “Boot Settings” which allow the user to set how the basic system will act, for example, support for PS/2 mouse and whether to use “Quick Boot” or not.

Table B-5 AMI BIOS Boot Menu



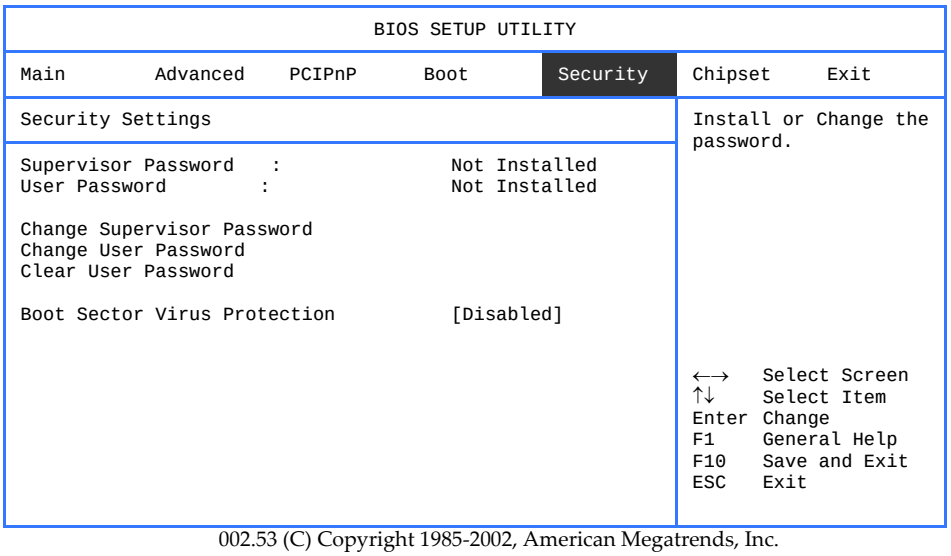
002.53 (C) Copyright 1985-2002, American Megatrends, Inc.

B.6 Security Setup Menu

The setup provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when setup is executed, using either the Supervisor password or User password.

Table B-6 AMI BIOS Security Menu



002.53 (C) Copyright 1985-2002, American Megatrends, Inc.

To reset the security in the case of a forgotten password you must clear the NVRAM and reconfigure.

Refer to Section **1.4.1** ***Clear CMOS/Password and BIOS Boot Mode*** on page 27 for instructions on clearing the CMOS.

B.7 Chipset Setup Menu

Select the various options for chipsets located in the system (for example, the CPU configuration and configurations for the North and South Bridge). The settings for the chipsets are processor dependent and care must be used when changing settings from the defaults set at the factory.

Below is a sample of the Chipset Setup screen; the actual options on your system may vary.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to Section **1.4.1** ***Clear CMOS/Password and BIOS Boot Mode*** on page 27 for instructions on clearing the CMOS.

Table B-7 AMI BIOS Chipset Menu

```
                              BIOS SETUP UTILITY
Main        Advanced    PCIPnP      Boot        Security    |          | Exit
-------------------------------------------------------------------------------
Advanced Chipset Settings                                   | NorthBridge chipset
                                                            | Configuration options.
WARNING: Setting wrong values in below section              |
         may cause system to malfunction.                   |
                                                            |
➢  NorthBridge Configuration                                |
➢  SouthBridge Configuration                                |
➢  Onboard Devices Configuration                            |
                                                            |
                                                            |
                                
```

B.8 Enabling and Disabling the Gigabit Ethernet boot-from-LAN BIOS

The Gigabit Ethernet boot-from-LAN BIOS provides support for booting over the network.

NOTE

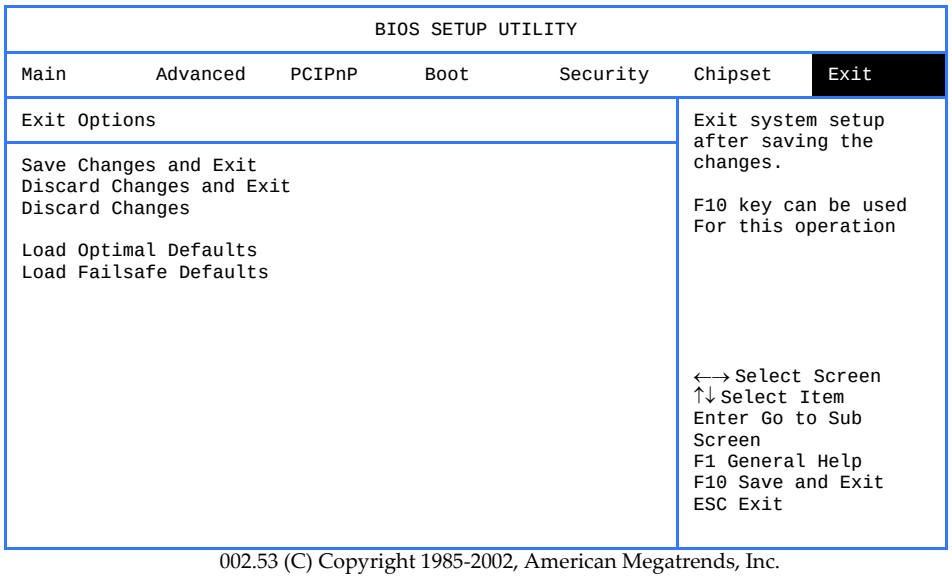
In order to boot from the network, some operating systems require that the network driver be set to "boot" within the Control Panel.

The Gigabit Ethernet boot-from-LAN BIOS defaults to Disabled in the BIOS Setup Utility. The *Chipset* menu of the BIOS Setup Utility allows the boot-from-LAN BIOS to be *Enabled* or *Disabled*. Table B-7 shows the *Chipset* Menu. Use the arrow keys to highlight the *Onboard Device Configuration*. Select 'GigE Option ROM' in the submenu's list and enter <+> until the option is set to *Enabled* or *Disabled*. Press F10 to Save and Exit the BIOS Setup Utility.

B.9 Exit Menu

Select the *Exit* tab from the setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the <Arrow> keys. The Exit BIOS Setup screen is shown below.

Table B-8 AMI BIOS Exit Menu



002.53 (C) Copyright 1985-2002, American Megatrends, Inc.

If changes have previously been made in the BIOS and the system malfunctions, reboot the system and access this screen. Select 'Load Failsafe Defaults' and continue the reboot.

C • Appendix C: Specifications and Physical Description

The V7875 operates from 5 VDC and the VME connectors are per VITA 1.7.

Table C-1 V7875 General Specifications

Characteristics	Specifications
Cooling Method	Convection
Conformal Coating	Optional
Operational Temperature	0° το 55° C (300 lfm)
Storage Temperature	-50° to 85°
Shock	20g peak sawtooth, 11 ms duration
Random Vibration	$0.002g^2$/Hz from 10-2000 Hz
Operational Humidity	Operating: relative humidity 5% to 95% noncondensing Storage: relative humidity 5% to 95% noncondensing
Altitude	Operating: 0 - 10,000 ft (3000m) Storage: 0 - 40,000 ft (12,000m)

© 2010 GE Intelligent Platforms Embedded Systems, Inc. All rights reserved.

* indicates a trademark of GE Intelligent Platforms, Inc. and/or its affiliates. All other trademarks are the property of their respective owners.

Confidential Information - This document contains Confidential/Proprietary Information of GE Intelligent Platforms, Inc. and/or its suppliers or vendors. Distribution or reproduction prohibited without permission.

THIS DOCUMENT AND ITS CONTENTS ARE PROVIDED "AS IS", WITH NO REPRESENTATIONS OR WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO WARRANTIES OF DESIGN, MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE. ALL OTHER LIABILITY ARISING FROM RELIANCE UPON ANY INFORMATION CONTAINED HEREIN IS EXPRESSLY DISCLAIMED.

GE Intelligent Platforms Information Centers

Americas:
1 800 322 3616 or 1 256 880 0444

Asia Pacific:
86 10 6561 1561

Europe, Middle East and Africa:
Germany +49 821 5034-0
UK +44 1327 359444

Additional Resources

For more information, please visit the GE Intelligent Platforms Embedded Systems web site at:

www.ge-ip.com

Publication No. 500-9300007875-000 Rev. D